April 2018

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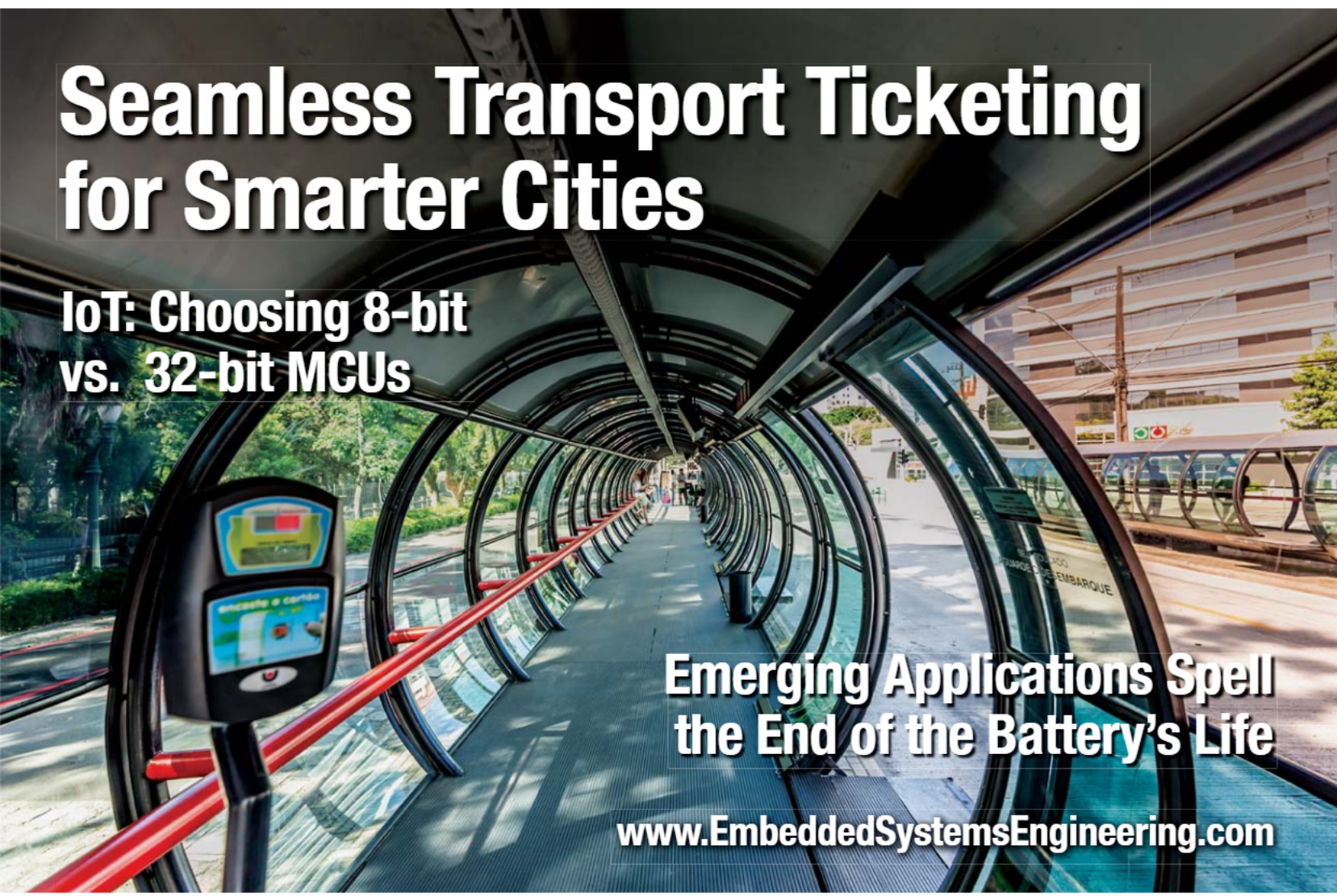

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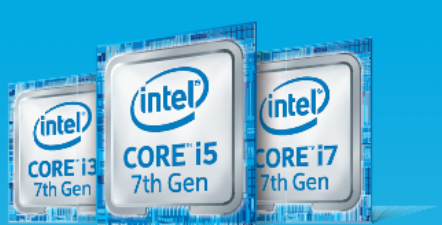

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How do Engineers Conserve Energy in IoT Devices? Let me Count the Ways…

Find energy savings in process technology, node scale, core architecture, hardware and software optimization, energy harvesting, and engineering grit.

By Lynnette Reese, Editor-in-Chief, Embedded Systems Engineering

IoT devices collect data through physical sensors, process sensor input on a low level (e.g., filter noise, discard unwanted data, etc.), a control scheme, or execute an action (e.g., local indication, alarm, fail-safe actuation, etc.), store data, and transmit data either via wire or wirelessly (i.e., telemetry). These functions consume energy.

Methods to reduce consumption can include using a low duty cycle, sampling data as infrequently as possible without affecting the validity of data interpretation. Keep circuits in a sleep state or off until needed. Circuits for wireless communication can be woken up to transmit a compressed data file and immediately put back to sleep. Power consumption can be unpredictable, as a core can consume different amounts of power at different times, depending upon the application. Using sleep power states can decrease power consumption but take progressively longer time for the CPU to act. A lower voltage supply will reduce energy requirements (P=VxI). However, supply voltage can be so low that external noise competes with true signals. Operating at a higher frequency can also save power, because more cycles can execute in the same period of real time. A drawback is that operating at higher frequencies can cause parasitics to increase, and more heat is generated. Another trade-off with operating voltages is that a higher frequency core necessitates a higher minimum voltage level. The challenge of lowest power consumption for computing power means more careful engineering with meticulous attention to detail.

Materials science also plays a role in balancing power consumption with higher performance. Ever-smaller technology scaling nodes have consistently lowered energy use but have become more complicated to implement. The core architecture and process technology make a difference in power consumption. Choosing the most power efficient architecture for a given IoT application is a challenge in trade-offs, as architectures offer different features. A newer process technology, Fully-Depleted Silicon-On-Insulator (FD-SOI), can optimize leakage in both active and standby modes, allowing one to adjust optimization for either power or performance dynamically, as needed.

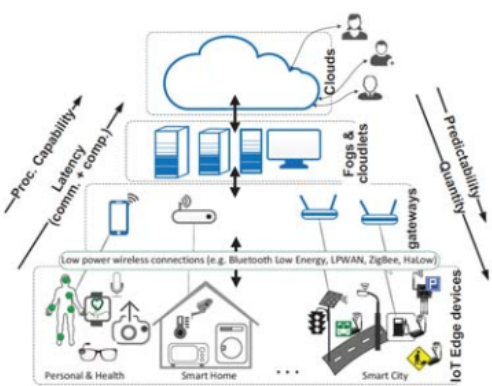

Figure 1: The layers of IoT computing and the communication between them. (Image: F. Samie, L. Bauer, and J. Henkel, "IoT Technologies for Embedded Computing: A Survey", in CODES+ISSS, 2016.)

Instruction Set Architecture (ISA) can affect power consumption, since some instructions can take more cycles to execute than may actually be needed. Software can be employed to optimize active modes by carefully managing or scheduling tasks. Compressing files for transmission so that the wireless circuit is active for the least amount of time also helps. "Race-to-idle" is a term that implies that execution should be sped up as much as possible so that execution (active) time is reduced (assuming that operating voltage is not adjustable.) One can also trickle-charge an IoT device via solar panels, harvesting byproduct energy from RF signals, or by converting rejected heat from a nearby device to energy.

Doubtless there are other ways to conserve energy, but the above illustrates several methods engineers use to lower power consumption. The real challenge is to select the best methods for your application and judge worthy design trade-offs, remembering that tactics in one area can affect your strategy in another.

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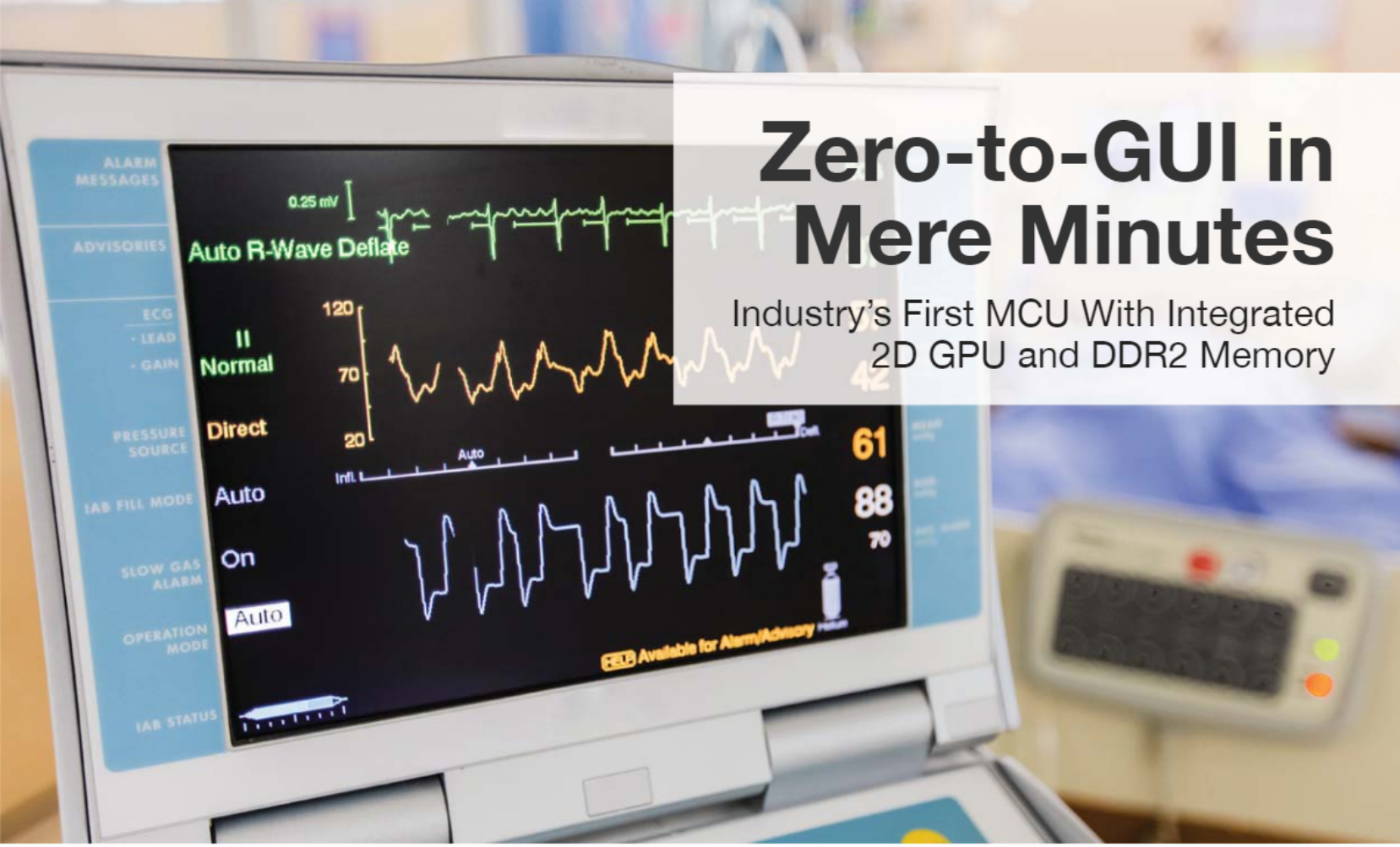

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What You Don't Know about Firmware Might Get You Øwn3d

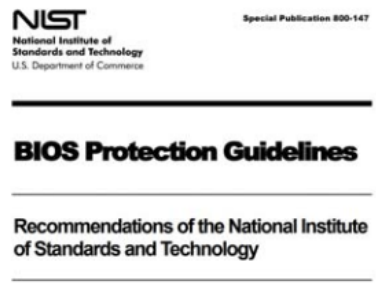
Making the first move to effective platform security takes a stronger understanding of threats to that security.

By Brian Richardson, Intel Corporation

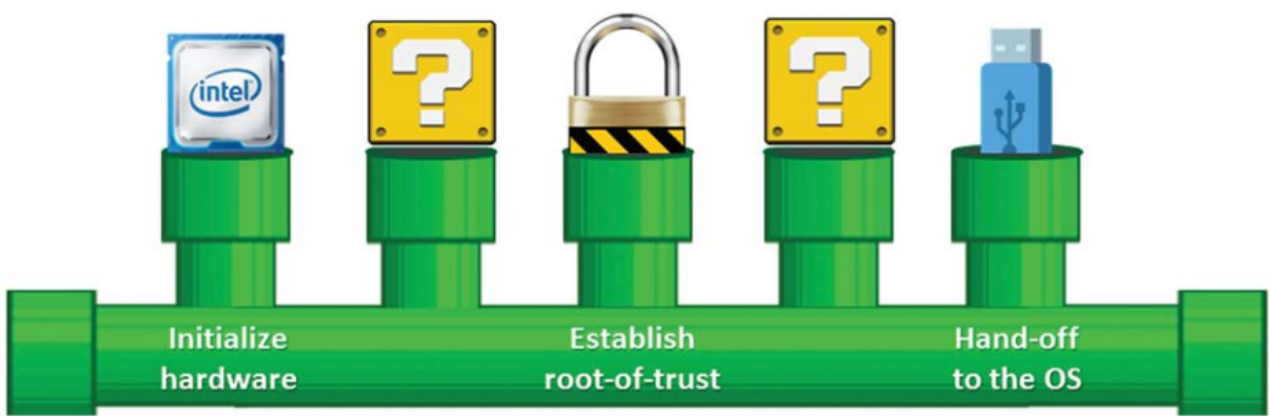
Technical marketing for firmware is an unusual job. When done properly, initializing the platform and launching an operating system should be an invisible process. Getting developers to notice something that should be invisible is tricky. It's a lot like plumbing: people don't appreciate how important it is, or how hard it is to do properly... until something goes wrong.

Unfortunately, there is an audience that has been paying more attention to firmware—computer security researchers —which is a fancy way of saying "hackers." A firmware attack may try to inject "stealthy compromise" code, bypass platform security features, or perform a denial of service by halting the boot process. Attacks operating at the firmware level can be difficult to detect, compromise software root-of-trust, and have the potential to persist across bare-metal recovery.

includes using UEFI Secure Boot to verify signed firmware components, using a Trusted Platform Module (TPM) to ensure platform integrity using security measurements, and delivering firmware updates via signed UEFI capsules.



The National Institute of Standards and Technology (NIST), part of the U.S. Department of Commerce, has created a series of "Special Publications" specifically for Cybersecurity (SP 800). A number of these directly address firmware security, including "BIOS Protection Guidelines" (SP 800-147) and "Platform Firmware Resiliency Guidelines" (SP 800-193). Microsoft provides a "Standards for a highly secure Windows 10 device" description. Developers use these guidelines to design new platforms, but IT professionals can also use these documents to create purchasing requirements based on best practices.



STANDARDS AND BEST PRACTICES

There are a variety of organizations developing guidelines for firmware. Most system firmware follows the Unified Extensible Firmware Interface (UEFI), which is a successor to the legacy 16-bit Basic Input/Output System (BIOS) popularized by the IBM PC/AT and its various clones. The UEFI Forum defines interfaces between the operating system and platform firmware, which include various security mechanisms. This

COMMON FIRMWARE ATTACKS

Attacks against platform firmware fall into three general categories:

1. Malicious code attempts to modify the operating system loader
2. Malicious code attempts to run from add-in components
3. Malicious code attempts to directly modify the platform firmware

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The first example, often referred to as a "bootkit" or "rootkit" attack, attempts to circumvent operating system protections by executing code during the hand-off from firmware. The most common vector is a modified boot media (SATA, SSD, NVMe, USB, etc.). The second attack is similar but uses modified Option ROMs on add-in peripherals (RAID, Network Card, Thunderbolt, etc.) to execute early in the boot process.

UEFI Secure Boot is designed to prevent the first two attacks exampled above by requiring that bootloaders and Option ROMs be signed against a known entity. This is typically the UEFI Certificate Authority (UEFI CA), but it can also be an operating system vendor or self-signed binaries for closed systems.

Attempts to insert code directly into platform firmware typically attack non-volatile storage on the Serial Peripheral Interface (SPI) bus. These attacks can be prevented by ensuring the SPI region is locked at runtime, which prevents programs from overwriting firmware contents and using signed capsule updates to prevent attackers from tampering with the manufacturer's firmware image. A TPM can also be used to detect tampering in all three cases, based on changes in measurements made during boot. Manufacturers also offer mechanisms like Intel® Boot Guard to preserve hardware root-of-trust.

Note that attacks may employ more than one method, such as a bootkit attempting to insert malicious code into the platform firmware during the bootloader phase. A comprehensive approach to firmware security employs multiple defensive methods.

DETECTING KNOWN ISSUES

CHIPSEC is an open source framework for analyzing platform security, with a focus on hardware and firmware configuration. CHIPSEC is a cross-platform security test suite with tools for forensics and low-level interface access. The utility detects issues based on common firmware configuration problems and publically available security research. CHIPSEC can also be used to generate a "whitelist" based on verified firmware or to create a "blacklist" to scan platforms for known malicious components.

While CHIPSEC isn't designed to be deployed on production systems, it is ideal for testing systems prior to deployment or during forensic analysis. New systems and platform updates can be scanned as part of pre-deployment testing or for periodic risk assessment.

KNOWING IS HALF THE BATTLE

Most of the work I do is working with other firmware developers to make sure they understand current capabilities and trends, but that work may take months or years to hit the market. The people on the front lines of computer security need some understanding of what they can do today to help secure their systems. Fortunately, there are practical methods to prevent a number of common attacks, platform security features to consider when purchasing new systems, and methods for detecting known firmware issues.

No computer system can be completely secure, but understanding potential threats is the first step to proper platform security. A better understanding of firmware and platform root-of-trust helps IT departments and penetration testing teams improve customer security.

In other words, you should know how the pipes work... just in case they break.

Brian Richardson is Technical Evangelist & Senior Technical Marketing Engineer at Intel.

He has spent most of his career as a "BIOS guy," working on the firmware that quietly boots billions of computers. He has focused on the industry transition to the Unified Extensible Firmware Interface (UEFI) and supporting the TianoCore open source community. Richardson has presented at various conferences and seminars, including Embedded Systems Conference, and is scheduled as a trainer for Black Hat USA 2018. When he's not talking about firmware at conferences, Richardson takes photos of his travels and procrastinates on various video projects.

Twitter: ***@intel_brian***
Blog: ***https://software.intel.com/en-us/meet-the-developers/evangelists/team/brian-richardson***

Home Efficient Home

How an RF smart plug can sweeten home energy savings by letting energy consumers see power consumption in context

By Salil Jain and Alok Kumar Mittal, STMicroelectronics

Salil Jain

With everything from refrigerators that help with grocery lists to secure doorbells that identify guests now connecting to the internet, energy consumption is soaring. However, solutions are coming online which make it possible to identify the energy usage of each device in relation to the whole and thus determine the most efficient timing and length of operation.

Alok Kumar Mittal

How would such a device work? It would need to be multipurpose, portable, and compact with the ability to measure and control electrical devices from any standard outlet in the home. It would need the ability to monitor energy consumption, turn appliances on or off, schedule loads for appliances such as clothes dryers and hot water heaters, and set alerts using easy smartphone apps.

Features necessary to successfully keeping an eye on power use and responding with actions that help maintain energy efficiency include:

- A meter design with wireless connectivity
- Bluetooth Low Energy (BLE) 4.1 connectivity for the control and metering panel as well as smartphone connectivity to enable the control of household appliances via an energy consumption dashboard
- The ability to control the loads of some appliances, including AC Induction fan speed, heaters, and incandescent lamps
- Scheduling
- A Near Field Communication (NFC) interface so that storing the logs to configure the design is possible
- Isolated USB interface for GUI and calibration: may be required during the development and calibration
- Rated voltage: 240 VAC, Rated Current: 12A (TYP)
- Power rating: Up to 2400W / 12 Amps
- Power consumption of plug: 0.7 Watts (Max.)

CONTROLLING CONSUMPTION

One example of a reference design that encompasses the above features is STMicroelectronics' RF Smart Plug for IoT home automation applications. It contains all the core functionality required for secure wireless communication, keeping energy consumption data in the user's control.

The smart plug is designed with the STM32L443 Microcontroller (MCU), based on the Arm Cortex-M4 core. This low-power MCU features crystal-less USB, 100 DMIPS, and an operating voltage from 1.71 to 3.6V.

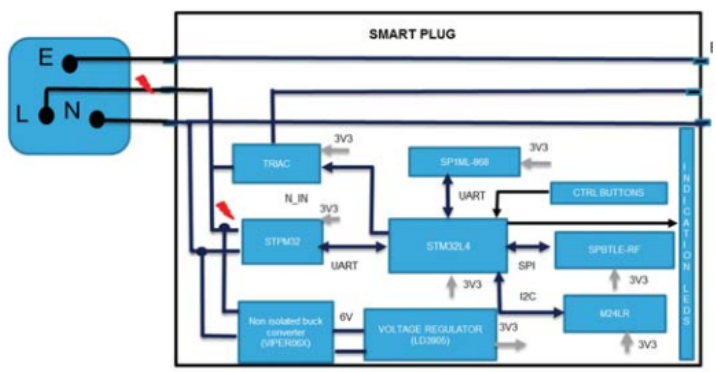

Figure 1: One example of device that facilitates power consumption measurement and control is the STMicroelectronics RF Smart Plug.

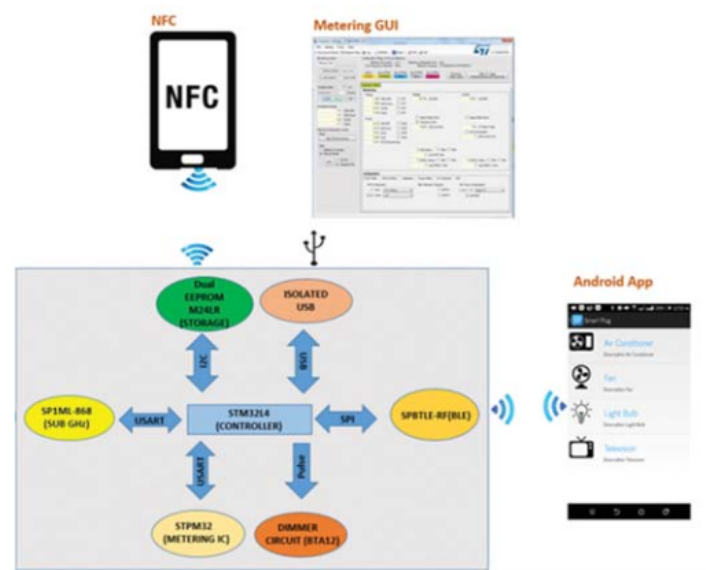

Figure 2: The STPM32 metering IC tracks power, voltage, current, and power factor parameters using wireless connectivity over SUB-GHz or BLE.

With wireless connectivity over SUB-GHz or BLE, the ability to measure energy parameters like power, voltage, current, and power factor is provided using the STPM32 metering IC (Figure 2). The MCU communicates with BLE using a Serial Peripheral Interface (SPI), with the help of the Triode Alternating Current Switch (TRIAC) to achieve load control. An isolated USB port and dual EEPROM (M24LR) allow communication with the Graphical User Interface (GUI) and Near Field Communication (NFC).

TWO MODES

The RF Smart Plug has two modes. In the first mode, the device acts as a BLE peripheral device, which can be connected for control along with monitoring. In the second mode, the device is a manufacturer-specific beacon, which is connectable. It advertises its metering parameters so that multiple Android smartphone brands can monitor the plug, but only the specific bonded device will be able to connect. This application runs at 48 MHz for optimal performance, while power consumption is in between 40 to 50mA.

Figure 3 highlights all the sections of the RF Smart Plug, showing how form factor and reliability challenges are met. This makes for a small, portable device, usable in any outlet in the home.

The non-isolated buck converter (Figure 4) is designed using STMicroelectronics' VIPER06Xs. It is used with Pulsed Wave Modulation (PWM) operation at 30 kHz with frequency jittering for lower Electromagnetic Interference (EMI), with standby power less than 30 mW. This type of power supply suits low current applications that demand a small form factor.

In our design, the output of supply is set at 4.5V. STMicroelectronics' LDO LD3905 voltage regulator is used to power up all the analog and digital sections with output voltage and current at 3.3V and 500mA, respectively.

CURRENT CONTROL

A Triode Alternating Current Switch or TRIAC is a three-terminal component used to control the current. It gives AC switching for various electrical system applications. In addition, it can change the duty cycle of the AC voltage applied to the lights/load being controlled. Figure 5 shows the status of AC voltage at 50% duty cycle and use of a Zero Cross Detection (ZCD) for a dimming reference point to fire the TRIAC.

Figure 6 explains the GATT and GAP role, and Figure 7 describes the State Machine of the RF Smart Plug.

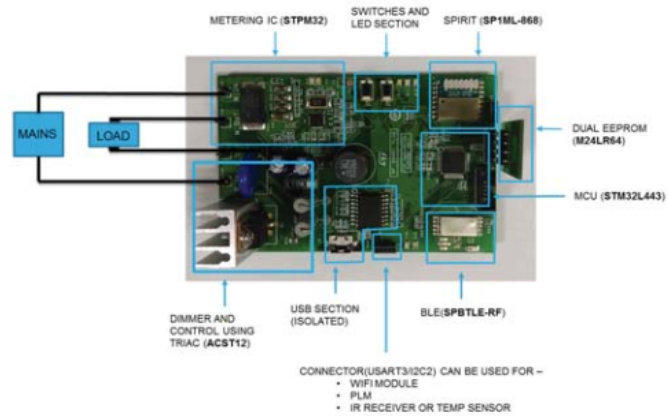

Figure 3: The two RF Smart Plug modes include: Bluetooth Low Energy peripheral device; connectable manufacturer-specific beacon.

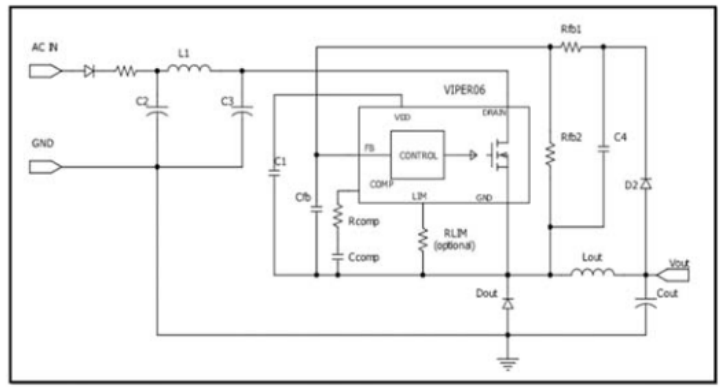

Figure 4: Non-Isolated Buck converter

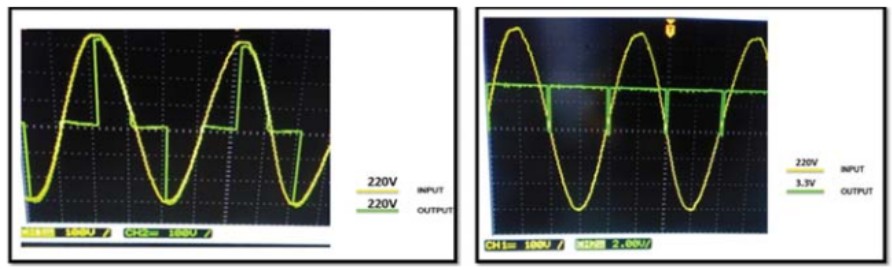

Figure 5: TRIAC at 50% duty cycle and ZCD

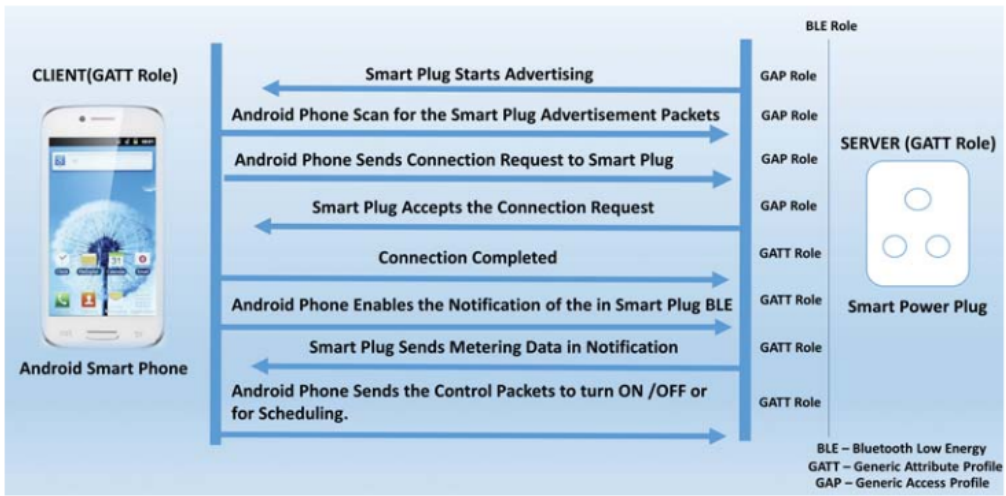

Figure 6: Functioning Principle

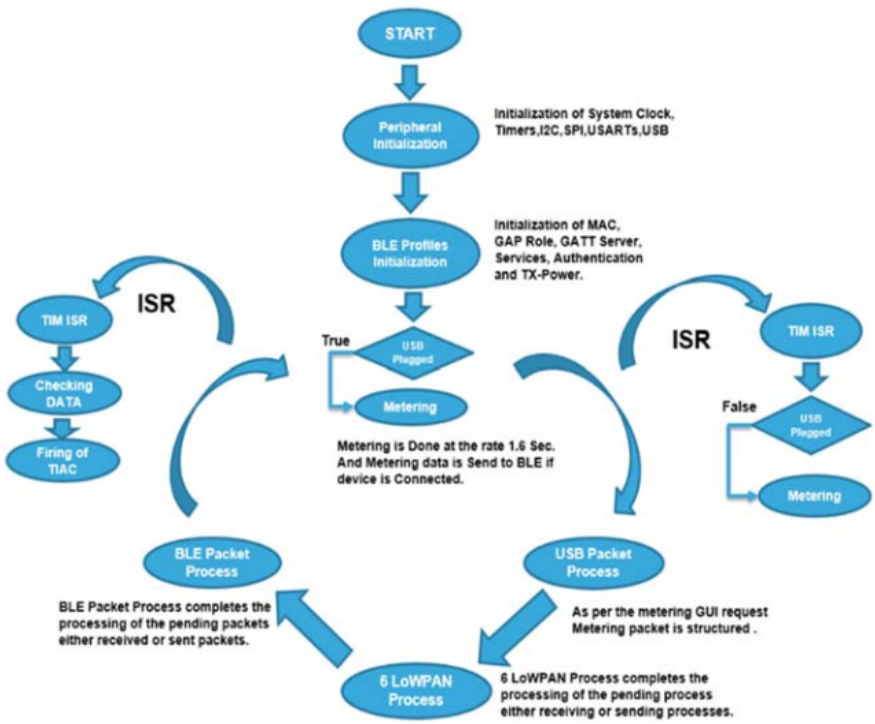

Figure 7: RF Smart Plug State Machine

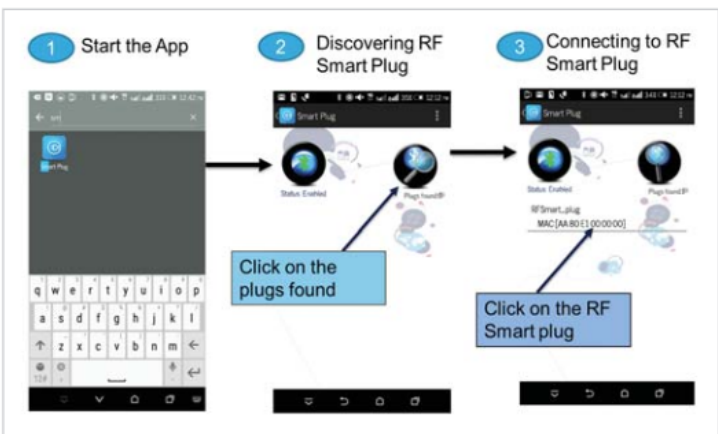

Figure 8: RF Smart Plug Android App

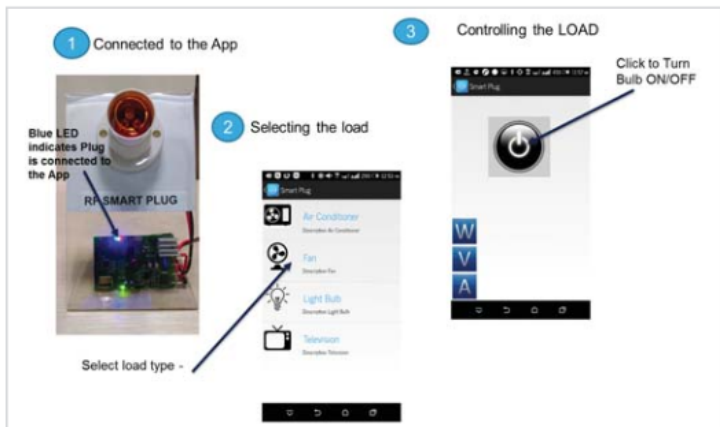

Figure 9: RF Smart Plug Android App Settings

ANDROID APPLICATION

An Android application designed by STMicroelectronics can be used for the Turn On/Off of the Load, Scheduling, and Dimming features.

The user can also view the metering parameters using the same application. The Android App can be downloaded by following the steps shown in Figures 8 and 9.

SUMMARY

This Smart Plug reference design is a system solution for energy management and saving with wireless connectivity over SUB-GHz or BLE. It provides the ability to measure energy parameters like power, voltage, current, and power factor using the STM32 metering IC. With all the core functionality required for secure communication, it provides a fast and flexible alternative to make homes smarter, money-wise, and safer.

Salil Jain is currently working as a Technical Leader with STMicroelectronics, and has seven years of experience as a designer, architect, and project leader of electronics systems for multi-disciplinary domains (HW & SW). His main area of interests are BLE Mesh, Metering, and Healthcare. He is the coordinator of IEEE under Special Education Initiative and is also the STM32 Microcontroller training member under e4i (Electronics For India) initiative.

Alok Kumar Mittal is currently working as a Group Manager with STMicroelectronics and has more than 20 years of experience in Embedded Systems Design. He has worked on applications around USB, mass-storage, energy metering, and wireless communication. His main responsibility includes architecture design of system solutions and their development, including integration with software applications. He has six patents granted to his credit. Currently, his area of interest is the BLE (Bluetooth Low Energy) Mesh solution.

Seamless Transport Ticketing for Smarter Cities

How migration from proprietary systems and the increasing prominence of open standards are making commuters' lives easier.

By Philippe Martineau, OSPT Alliance

The world's cities are growing at a phenomenal rate. It is estimated that by 2050, 66% of the world's population—a staggering 6.419 billion—will be living in urban areas. With this rise come two main developments. One, city services such as the transport network must be capable of serving greater numbers of passengers quickly, effectively, and securely every day. Two, with growing urban populations comes greater connectivity. Combined, this amounts to an even greater demand for smarter, more seamless operations to ease the consumer's day-to-day life, facilitated by advances in technology.

Cities are getting bigger, more connected and crucially, smarter.

South America is one region currently experiencing such rapid urban development. In an attempt to deliver a more frictionless service to its rising number of smart city travellers, the transport ticketing ecosystem in the country is in the process of upgrading and restructuring.

LEGACY AND OTHER OBSTACLES

Despite a sincere desire to support innovation and deliver superior experiences for passengers, transportation agencies have had to overcome significant legacy obstacles to deliver any considerable advances. Throughout the market, in South America and beyond, operators are bound to customized proprietary fare collection systems from a single-source supplier.

As a result, accommodating new technologies and the costs to upgrade systems are dictated at the pace and the price of the incumbent vendor. The dominance of proprietary systems in the transport ticketing market, and the lack of ownership of the ticketing specifications by the transportation agencies is, undoubtedly, the central factor hindering innovation.

TRANSFORMATIVE

Standardization, as it has done across industries such as IT and telecoms, can have a transformative power. In transport ticketing, it can level the playing field and be the key to driving effective, sustained innovation. One example of a non-proprietary standard is CIPURSE™, which is developed and managed by OSPT Alliance, a member-driven industry association. CIPURSE is fully configurable and adaptable to the requirements and innovations of the transit ticketing community.

SIMPLER

Operators with infrastructures built on proprietary systems must wrestle with costly, complex upgrades to their systems when accommodating each emerging payment form factor and/or security scheme. Standardization simplifies these complexities.

Built on the international smart card command (ISO 7816) and interface (ISO 14443) standards in conjunction with AES security (FIPS 197, ISO/IEC 18033-3), CIPURSE supports each fare media device with the same security protocols. This means there is no need to upgrade CIPURSE compatible readers and terminals when incorporating new ticketing formats—whether that's adding in mobile

Figure 1: Arguably the smart city's nervous system, its transportation network is stepping up with the help of open standards to meet the needs of more and more travelers quickly, effectively, and securely every day.

ticketing acceptance or accommodating wearables, CIPURSE also offers the interoperability and scalability to simplify this process into adjacent markets and services.

RAISING THE GAME

With open standards, technology benefits from increased innovation, too. Working collaboratively, OSPT Alliance's member organizations share a vested interest in sustaining and advancing standards. Operators have the freedom to select the best vendors and business models for their solutions, which in turn offer new players a greater opportunity to showcase their offering, promoting healthy competition in the industry.

Let's take a closer look at how CIPURSE is driving projects forward in South America.

MITIGATING FRAUD AND ERRORS

The mature and secure CIPURSE standard offers an answer to mitigating losses due to fraud, system errors and cash handling. In addition, with some big cities in Brazil, for example, passengers may need up to three cards for travel. CIPURSE's interoperability enables all three cards to be combined into one. The benefits for the consumer are obvious, but this saves the operators a number of logistical headaches and costs, too.

However, hesitancy persists surrounding the supposed high costs and complications of replacing proprietary systems. Experience has now shown this 'rip and replace' overhaul is a myth, and one that Brazil-based OSPT Alliance member Planeta Informática is keen to dispel.

Planeta Informática's mission is to support transport players across the continent to begin the process of migration from proprietary solutions to the benefits of open standards, offering 'off the shelf' CIPURSE solutions and consultancy support to system integrators and transport operators.

As neither the ticket data nor the back-office system must change to enable CIPURSE deployment, upgrade costs are minimal. A small secure application module, or SAM, simply needs to be integrated into the gates and validators of the system to add recognition of CIPURSE into existing systems.

Planeta Informática has been an industry-leading SAM provider for the last 10 years, with more than 200,000 SAM devices currently deployed, supporting 30 million users per day across South America. Utilizing virtualization technology, its latest SAM device enables the simple integration of CIPURSE into existing systems without having to change the current application software, validator software, or host system. Plus, as CIPURSE can operate alongside legacy solutions, a phased, cost-effective approach to card replacement can be taken, as existing cards can continue to be used.

MINUS PAIN, RISKS, COSTS

It's with this simple approach that Planeta Informática has launched what's set to be the largest scale CIPURSE deployment project to date in Cuenca, Ecuador. With the deployment now complete, it is expected that a full migration to CIPURSE card usage will be in place before the end of 2018. By then, the project will see over half a million CIPURSE-based contactless cards introduced without the pain, risk or costs of upgrading to a proprietary solution.

Open standards enable flexibility to scale up operations simply and cost-effectively. And with interoperability across all sections of the ecosystem, services are safeguarded for the future. Looking longer term, this simple upgrade to the system enables operators to remain flexible when looking to integrate mobile ticketing or account-based ticketing solutions, for example.

Now in operation on more than 500 buses and across 300 terminals, with minimal disruption to passengers and safeguarded investment in legacy hardware, Cuenca is already beginning to reap the benefits of open standards whilst remaining fully open to future advancements.

Open, non-proprietary standards are changing the game. In short, enabling more secure, cost-effective, scalable, and extensible transit fare collection systems that benefit both the transport stakeholders and the end traveller.

WHO IS OSPT ALLIANCE?

The OSPT Alliance is an international association chartered to provide the standard for secure transit ticketing solutions and beyond. It provides industry education, creates workgroup opportunities, and catalyzes the development and adoption of innovative fare collection technologies, applications and services. OSPT Alliance membership is open to technology providers, transit operators, consultants, solution vendors, government agencies, reader and terminal manufacturers, system integrators and other stakeholders in the contactless ecosystem.

Through the work of its members, the Alliance aims to promote CIPURSE implementation worldwide. For additional information, please visit www.osptalliance.org.

Philippe Martineau is President of the OSPT Alliance Board. He is a seasoned international executive who has worked most of his career in the extended Mobile eco-system. His career started with the emergence of the mobile technology in the early '90s where he contributed to GSM standardization, bringing the SIM technology to market. Doing so, he has developed a strong knowledge of the operators' ecosystem through 17 years at Gemplus with roles ranging from R&D engineering, head of the Telecom business unit to VP of Strategy.

He has since contributed to bringing innovative technologies to market such as NFC as Executive Vice President of INSIDE secure NFC Business line. Having worked for both startups and larger enterprise, he has developed an acute sense of business acumen to combine technology understanding with pragmatic go to market strategies. Martineau is now Senior Director of ecosystem Business development in the CTO office of Rambus where his role consists in bridging Rambus core technology with the mobile world. He has also recently been appointed Chairman of the OSPT Alliance with the intent to drive a greater momentum in the definition of Mobility services.

IoT: Choosing 8-bit vs. 32-bit MCUs

It's generally known that 8-bit MCUs have an overall advantage over 32-bit MCUs in physical size, power efficiency, and cost. But do 8-bit MCUs have what it takes for IoT?

By Lynnette Reese, Editor-in-Chief, Embedded Systems Engineering

Do 8-bit microcontrollers fit in the Internet of Things? In 2015, 8-bit microcontrollers (MCUs) still held more than 35% market share of global microcontrollers, according to Allied Market Research.[1] On Mouser.com (an electronics distributor with a large selection), there are nearly triple the number of 8-bit MCUs to choose from compared to 32-bit MCUs. Clearly, 8-bit is not dying. There remains a very large selection of 8-bit MCUs offered by NXP, Microchip, Silicon Labs, Analog Devices, Renesas, Texas Instruments, Cypress Semiconductor, and several others. The 8-bit MCU has had a 30-year head start over 32-bit MCUs and is entrenched in existing embedded systems where control, not processing power, is the primary focus. While 16-bit MCUs remain in the picture, the extremes in specifications, features, and benefits are best observed in a comparison of 8- and 32-bit MCUs.

A little over a decade ago, 32-bit MCUs began their ascent to dominance as prices decreased while performance increased. These traits, combined with decreasing power consumption, have made the 32-bit MCU irresistible, enabling us to put 32-bit MCUs in everything from watches to refrigerators. The Internet of Things (IoT) is a deluge of smart, data-collecting, decision-making devices that contribute to an informed world; a world where we can more accurately predict anything that can be precisely trended. The IoT promises to improve productivity with more accurately aimed decision-making in several markets, including Automotive, Agriculture, Industrial, Healthcare,

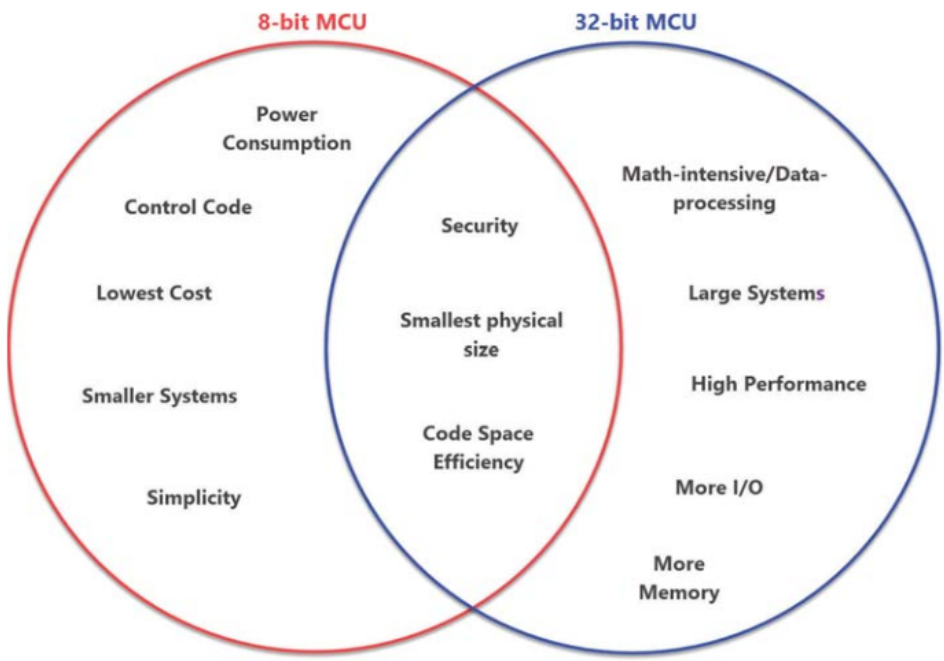

Figure 1: Venn diagram of the 8-bit MCU vs. 32-bit MCU benefits from a general perspective, as direct comparisons of all features combined are relative to tradeoffs. In general, the 8-bit MCU has been lower cost and smaller in size than the 32-bit MCU, but 32-bit MCUs are close to competing on cost and both have at least one "specimen" of a similarly minute physical size. In overall power consumption, the slower 8-bit MCUs will always trump the faster 32-bit MCUs as long as manufacturers stay on their game.

Simplifying 16-bit PIC® Microcontroller Designs

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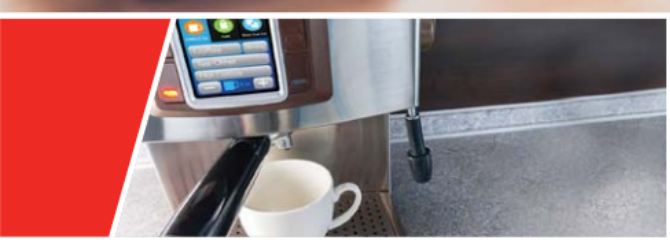
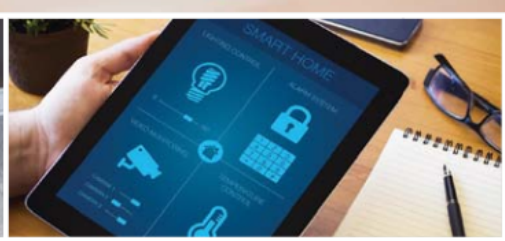
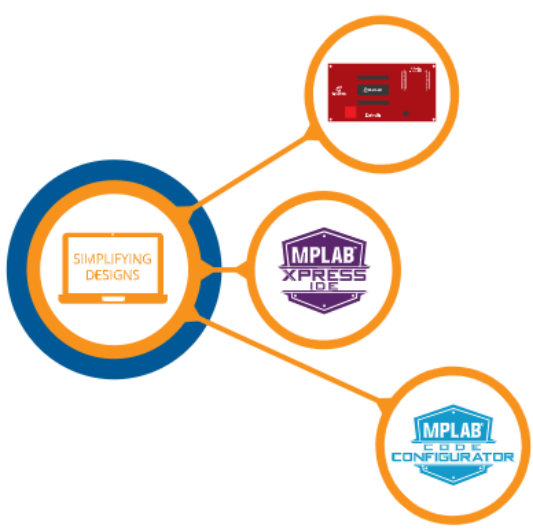




Are you new to 16-bit PIC microcontrollers or starting a new design? Step into the world of unlimited possibilities through an easy-to-start ecosystem including the PIC24F Curiosity Board, MPLAB Xpress Cloud-based IDE and MPLAB Code Configurator (MCC) to simplify your designs. This trio of tools can jump-start your design by facilitating creation of your prototype design.



1. **PIC24F Curiosity:** Rapid prototyping board for only $25
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3. **MPLAB Code Configurator:** Intuitive code development tool for PIC24 MCUs and dsPIC33 DSCs

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and Consumer devices. Supply chains will also reap rewards in the form of nimbler logistics, shorter time-to-market, reduced costs, increased employee (and personal) productivity, and more satisfying customer experiences.

IOT AND THE 8-BIT MCU

To qualify as IoT, the most basic of devices need only include a secure processor, a cloud, and some means of communicating data over the internet. However, the low cost, low power consumption, and small physical size of the 8-bit MCU are still compelling in applications that predominantly require simple control code over processing power. A device that reads a few sensors and controls a process will suffice with an 8-bit MCU, even as an IoT application. (IoT is broadly defined, after all.) More sophisticated requirements that require high-performance, more memory and a larger number of I/O often require a 32-bit MCU or even a 64-bit processor. Some IoT devices have enough processing power to make local decisions, termed "edge computing," which avoids sending massive amounts of raw data to the cloud.

MAKING THE CHOICE BETWEEN 8-BIT AND 32-BIT

It's generally known that 8-bit MCUs have an overall advantage over 32-bit MCUs in physical size, power efficiency, and cost. The project itself, or system requirements, will dictate what is necessary, but in a gray area concerning trade-offs between 8- and 32-bits, then either MCU is likely suitable. If you have the time to investigate your use cases, the MCU that could make life easier might show in the details. In that case, there are several areas to look at in determining what's best for your system.

IN BLACK AND WHITE

First, examine your system requirements in several areas. In some cases, it's clear that an 8-bit MCU will suffice, especially if the final program can fit into less than 8 KB of memory, and budget dictates under 50 cents per unit. An 8-bit MCU will likely suffice if your system, along with code and data size, is small, and cost, physical size, and power consumption are large factors. An 8-bit MCU can be as small as Microchip's (Atmel) ATtiny20-UUR at a package size of just 1.5 mm x 1.4 mm. Pushing up to 12MIPS at 12MHz, the ATtiny20 is IoT-ready with ultra-low power consumption at 200µA in active mode, 25µA in idle, and 0.1µA in power-down mode.[2] In comparison, the 32-bit NXP Kinetis KL03 is not far off; at a small 1.6 mm x 2.0 mm in a WLCSP-20 package, the 48 MHz ARM® Cortex-M0+™ has "run power consumption as low as 50 µA/MHz."[3] Both have I2C and SPI. Amazingly, each is priced similarly. The non-monetary price for 32-bit performance works out to a physics problem: pushing more bits at 4x the speed consumes much more power. If battery life is a concern and you are in the gray area, you might find 8-bit MCUs irresistible.

Systems with a need for more I/O, larger programs (> 64KB of code), or larger data memory (> 256 KB) will gravitate beyond what 8-bit MCUs can provide. (Choices in 8-bit MCUs begin to thin out at a data memory size over 256 KB.) High-performance processing with math-intensive computations or a requirement for fast data manipulation belongs to 32-bit and higher.

Don't forget to look at the simplicity factor. The simplicity of 8-bit MCUs has created a following; 8-bits is a lot easier to work with than 32-bits on several levels. Following the software and hardware on an integrated level at 8-bits is simpler than at 32-bits. Development tools can be a decision-maker in that free tools may not be available for a particular MCU. The cost of paid tools can be anywhere from a few hundred to a few thousand dollars per seat. Free, open source tools are worth checking out. The level of community and forum support for your MCU of choice may also have weight, depending on how much personal support you believe the manufacturer will provide. Documentation matters, as well, in terms of the frustration factor. If documentation is sparse, look for extremely active and supportive forums, otherwise, that should be a mark against an MCU in competition for your business.

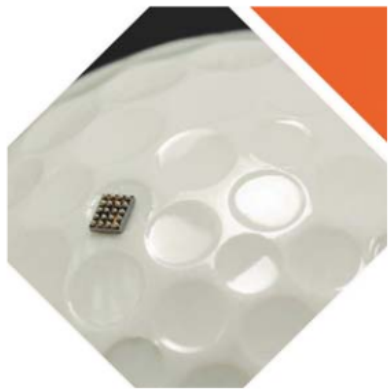


Figure 2: The NXP Kinetis KL03 20-pin ARM® Cortex®-M0 powered MCU, at 1.6 mm x 2.0 mm, is suitable for ingestible healthcare sensing. The KL03 (MKL03Z32xxx4) supports 32 KB Flash, 2 KB SRAM, 8 KB boot ROM, and up to 22 GPIO.

SECURITY

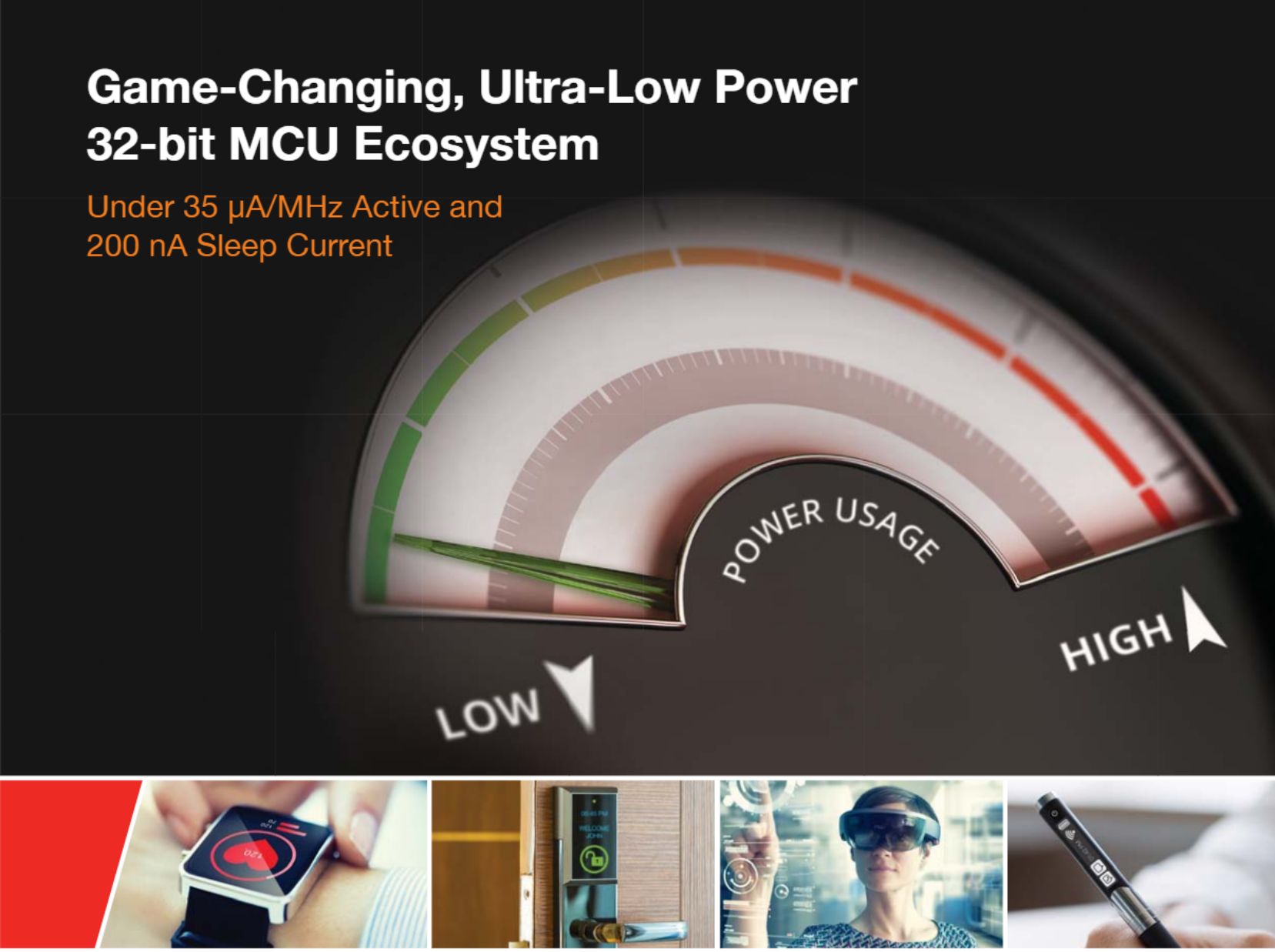
After you have considered the above and you are still on the fence between 8-bit and 32-bit, determine what kind of security is needed. Security begins at the silicon. External security chips, if installed at all, are vulnerable at the connection point. What security options will you have for your IoT device? Ideally, it should be integrated into the silicon, such as ARM's TrustZone®, which can simultaneously run a secure operating system (OS) and a normal OS on the same core. TrustZone is designed for protection over a wide span of assets. The 8-bit MCU may provide some cryptographic support in software or external devices, but external security hardware increases costs and security implemented in software creates the burden of extra overhead.

THE LARGER THE SYSTEM...

Last, you can look at the finer details of processing, perhaps comparing latency if real-time is on your requirements list. Superiority in low-latency does not necessarily belong to 32-bit MCUs, however. The details depend on the use case. Issues like delays in an interrupt service routine of a larger system can become insignificant as execution time increases, as witnessed by Josh Norem of Silicon Labs, who did a comparison of an ARM core with an 8051. Norem states, "In keeping with the established theme, the larger the system gets, the less the 8051 advantage matters."[4] Norem's fairly detailed comparison between a 32-bit ARM Cortex and an 8051 led Norem to find that in many cases, the detailed differences between the 8-bit 8051 and the 32-bit ARM-core MCU related back to overall system size: larger systems trend towards requiring 32-bit MCUs.

Game-Changing, Ultra-Low Power 32-bit MCU Ecosystem

Under 35 µA/MHz Active and 200 nA Sleep Current



Microchip's ultra-low power and low-power MCUs balance power consumption and performance to meet the needs of a wide spectrum of power-constrained applications from wearables to IoT nodes. These MCUs are designed from the ground up utilizing low-leakage processes and libraries to provide industry-leading low power consumption in both Active and Sleep modes.

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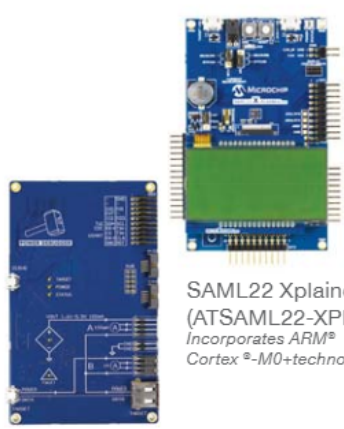

SAML22 Xplained Pro (ATSAML22-XPRO-B)
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Before casting away the humble 8-bit MCU, however, make note that makers of 8-bit MCUs have not been twiddling their thumbs; over the past 30 years, many advances have been made to 8-bit MCUs. Today's 8-bit MCUs sport advances in security, wireless connectivity, ultra-low power consumption, integrated features like analog-to-digital converters, modules, Analog Front Ends (AFEs), and other advanced features.

Microchip's 8-bit PIC18F65K40 MCUs include Core Independent Peripherals (CIP), which bypass the processor to deal directly with other peripherals. According to Microchip, "Core Independent Peripherals are designed to handle their tasks with no code or supervision from the CPU to maintain operation. As a result, they simplify the implementation of complex control systems and give designers the flexibility to innovate."[5]

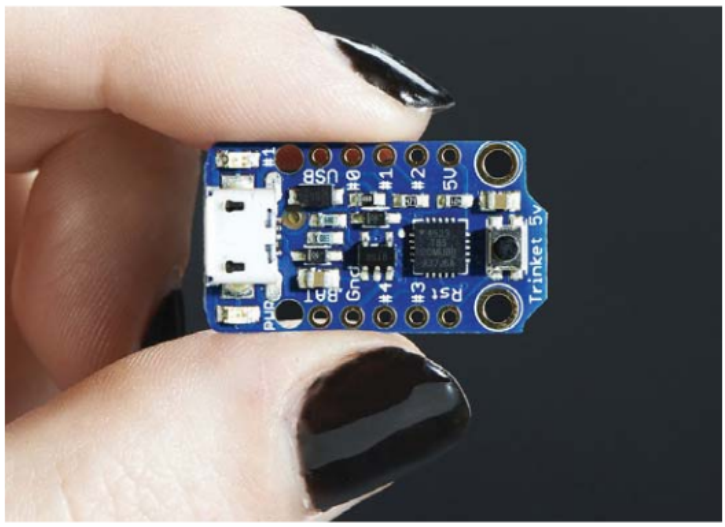

Figure 3: Adafruit's Trinket board comes mounted with a Microchip ATtiny85 MCU, 8KB of flash, and 5 I/O pins, including analog inputs and PWM 'analog' outputs. At a tiny 1.2" x 0.6" x 0.2" (31mm x 15.5mm x 5mm), it works with free Arduino IDE tools. (Source: adafruit.com)

ADDITIONAL CONSIDERATIONS

The 8-bit MCU moves fewer data at a time than the 32-bit MCU. Will you be moving a lot of data around? Does your natural data set size match the MCU data width, or will you be converting every line of 32-bit data for 8-bit consumption? Be aware that the 8-bit system is simpler to work with overall. Development tools play a part, but in general good tools are available for MCUs in both categories. The more complex 32-bit MCUs can handle more variations on peripherals, but with more features comes more complexity. Fewer moving parts are best for beginners, especially if you want to really get deep into how it all works together. Keeping your distance from the hardware with neat, well-behaved layers of abstraction is not always an option, however, so make complexity a deciding factor, all other things being equal.

It's a good thing that the 8-bit MCU market doesn't show signs of slowing down, as many maker-level (DIY) projects are very accessible to tinkering with just about everything at 8-bits (see Figure 3). The 32-bit MCU is probably a better choice for a certain class of IoT devices that process data before sending it to the cloud. The market is fluid, and 8-bit wins often for IoT devices that must sip power as a top priority, but nothing says that one 32-bit device cannot process the raw data from several 8-bit IoT devices locally before pushing it up to the cloud as an edge device.

In short, know your system requirements well, including the budgeted cost, the power budget in several MCU states, and how long the MCU might reside in each state. Have an idea of any physical size limitations, the level of security desired, and where the MCU will be spending most of its time: on control code/general processing or computational/math intensive processing? Security has become a concern in recent years as internet connectivity has opened the door to hacking, adding an additional burden in overhead for all MCUs. As for 8-bit MCUs powering IoT devices, it's likely we will see more 8-bit MCUs as "accidental IoT" as some systems get implemented with remote communication via the internet for convenience.

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Lynnette Reese is Editor-in-Chief, Embedded Intel Solutions and Embedded Systems Engineering, and has been working in various roles as an electrical engineer for over two decades. She is interested in open source software and hardware, the maker movement, and in increasing the number of women working in STEM so she has a greater chance of talking about something other than football at the water cooler.

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Adding Intelligence to Fixed Function ICs: Q&A with TI

A low-cost entry point approach to simple sensing applications

By Anne Fisher, Managing Editor

Dave Smith, Texas Instruments

Editor's Note: The announcement that Texas Instruments (TI) now offers its ultra-low-power MSP430™ microcontrollers (MCUs) at around 25 cents in high volume made for a good occasion to speak with Dave Smith. Smith is the Product Marketing Manager for TI's MSP430 FRAM-based microcontrollers and argued that there are Big Reasons for Small MCUs in an earlier article. Now, Smith explains that reasons for designer interest in the MSP430 line go beyond just the low-price entry point. Edited excerpts from our conversation follow:

EECatalog: What comprises the MSP430 Value Line Sensing MCU family?

Dave Smith, TI: This is a collection of application reports complete with code libraries aimed at adding a little bit of intelligence to fixed function ICs—that is, some of the common things found on a PCB: comparators; real-time clocks; EEPROMs; supply voltage supervisors; reset controllers—some of the simple functions that many PCBs have.

EECatalog: What goes into the decision to use a microcontroller rather than an off-the-shelf product?

Smith, TI: When thinking about the decision to use a microcontroller as compared to an off-the-shelf product you're often looking at a situation where there is not an exact fit for one of the off-the-shelf products. In those cases, using a microcontroller can enable an engineer to tailor the functionality, whether a simple timing parameter or a particular sequence of wake up events, for example, to their application needs. However, we are not trying to go head-to-head with an off-the-shelf whatever-type IC, but rather adding to that.

EECatalog: Could you offer an example?

Smith, TI: Yes. Things like a real-time clock or a system wake up controller is where we are targeting some of these applications or these functional blocks. So, while I can buy an off-the-shelf real-time clock, what I can't buy is something that really fits in with the system needs that I have. In this case we are using the FRAM nonvolatile memory along with the real-time clock and allowing them to use that as a combination of real-time clock and EEPROM.

Another example is a programmable system wake up controller. Yes, I can buy an external chip that is going to trigger a wake up every 100 milliseconds, two hundred milliseconds, whatever is hard-wired into that part. With the MSP430 based solution we can adjust the sleep interval and wake up schedule by simply sending a command over the UART, this added flexibility can help to extend system battery life.

Or say I have an RF chip, Bluetooth, Wi-Fi or whatever, but I want it in a battery-powered system, some home security product or network product. I may not want that to be active all the time because I want the battery to last more than six months, 12 months. With this type of device, I can program it so that it only wakes up that RF chip when something relevant happens—that could be monitoring an ADC for example.

In the low-power MSP430 we can monitor an ADC or use the window comparator to significantly drive down the power consumption of that overall system. Many of those functions could be incorporated into the main logic processor, but it is often very inefficient to do that. So, it may be a part that may have low-power modes and may be able to go into some of the shut-down modes but may be limited or use even more power when it is in those modes, than the MSP would.

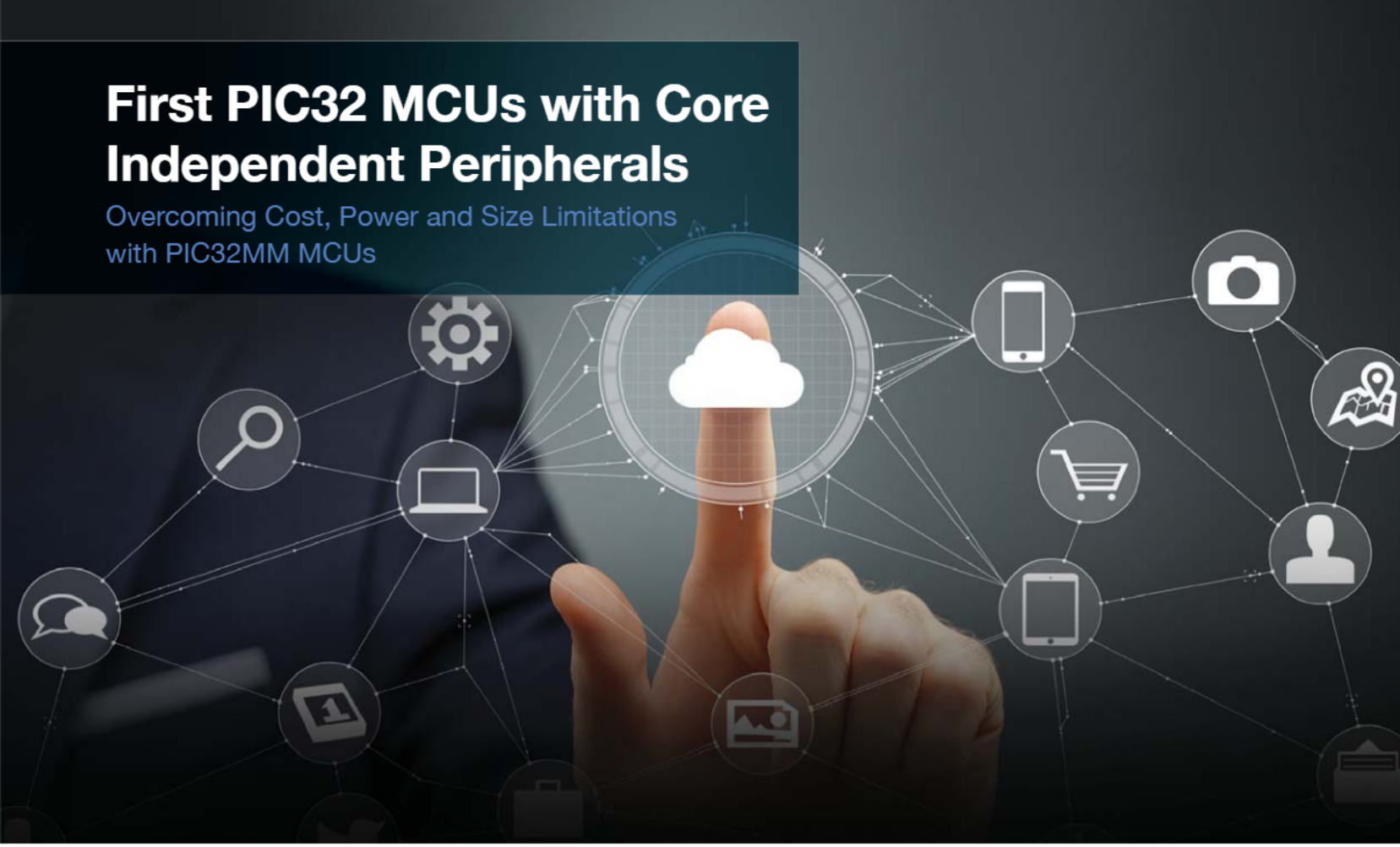
EECatalog: So designers can hew a bit closer to their application's demands than they might be able to with an off-the-shelf IC?

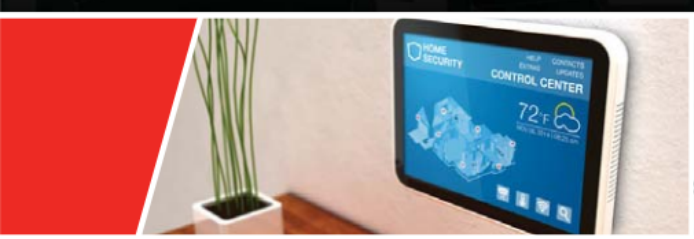
Smith, TI: Yes, we see a lot of customers that are trying to develop energy harvesting or maybe scavenging applications where the ability to do very low power stores, or nonvolatile stores, or operate for longer with a very limited power supply. Whether that's a rechargeable battery that is charged by solar panels or just a conventional battery, lasting longer between service intervals will help to reduce maintenance costs and overall system ownership costs.

A couple of other examples: On the PWM one of the example code snippets creates a dual 8-bit DAC, so in a standalone situation this

First PIC32 MCUs with Core Independent Peripherals

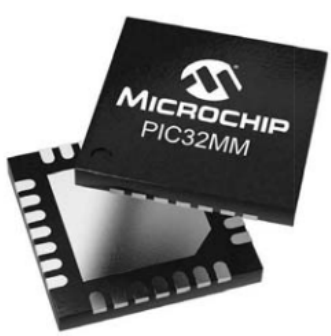
Overcoming Cost, Power and Size Limitations with PIC32MM MCUs





As the first PIC32 microcontrollers to offer Core Independent Peripherals, the PIC32MM family delivers cost-effective, low-power embedded control for IoT, consumer, industrial and sensorless BLDC applications.

The Core Independent Peripherals, such as Configurable Logic Cells (CLCs) and Multiple Output Capture Compare PWMs (MCCPs), offload tasks from the CPU to deliver lower power consumption and lower design complexity. Additional power savings, enabled by low-power sleep modes, plus small, 4 × 4 mm package options support longer battery life in space-constrained applications.



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could be a simple sounder. Maybe it gets a push button or some other trigger from an ADC or a comparator and then it plays a tone or a series of tones to indicate that something has happened. Everything from a simple doorbell to a simple timer.

Or it could be incorporated into a larger system, where you are going to send some communication data, some serial data, to trigger that signal. So that's a little dual DAC. It could be as simple as controlling color blending on an RGB LED.

Figure 1: Smith notes the applicability of microcontrollers that allow the customization of system-level functions to markets such as Smart Home. (Courtesy TI)

One of the areas that we have really seen this being taken up by our customers is where they are looking to do very low power nonvolatile writes. With an energy-harvesting solution or with a small coin cell battery, if you need to write data in a conventional flash or EEPROM memory the mA's of current required will quickly deplete the available stored energy. Conventional EEPROM and Flash technologies include a charge pump within the device that is required to boost the supply voltage to a higher voltage. It takes timing to do that and, more critically, it takes a significant amount of energy to do that.

If you want to store something in a system whether sensor data or whatever data it is—and want to store it frequently—that can quickly deplete the battery. The FRAM technology we're using with the MSP430 Value Line is very, very low power. We don't have the charge pump involved, which also makes it faster.

It's also very high erase/write endurance, with 1015 cycles as compared to the typical 100K or 1M cycles of EEPROM or Flash.

EECatalog: What are you seeing in the ecosystem of folks coming up with interesting sensors?

Smith, TI: We see a lot of activity in and around the connected home. Yes, there is a lot of activity going on in office and factory automation as well, but the home automation that is going on at the moment and is driven by cloud services and the big names rolling out the personal assistants stands out.

The automation being built into homes is going into places that I don't think even a couple of years ago we would have expected to see that level of intelligence, whether through some of the simple applications we have been talking about here, or things that use capacitive touch to program thermostats or to operate a voice assistant just to trigger something. I think where we are going to see explosive growth is in the home automation, small appliance, and personal assistant areas, and these parts can definitely play roles in that because many of these are battery-powered. Longer battery life makes battery changes less frequent and helps the environment.

EECatalog: Are there some additional things our readers should know before we wrap up?

Smith, TI: These half-a-kilobyte to 1-kilobyte in FRAM devices also have half a kilobyte in SRAM, and this is one of the characteristics which sets them apart from competitive devices. Usually if you have a small program memory, you will have a very small data memory. With the competitions' 512-byte program memory, you might get 64 or 128 bytes of data memory.

In our parts, if you get 512 bytes of program memory, you actually get 512 bytes of data memory as well, so that makes it a little more programmer friendly; it allows you to do more with the device.

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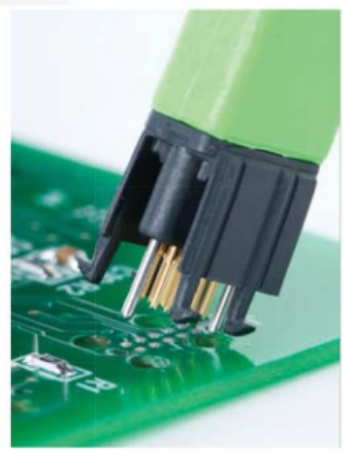

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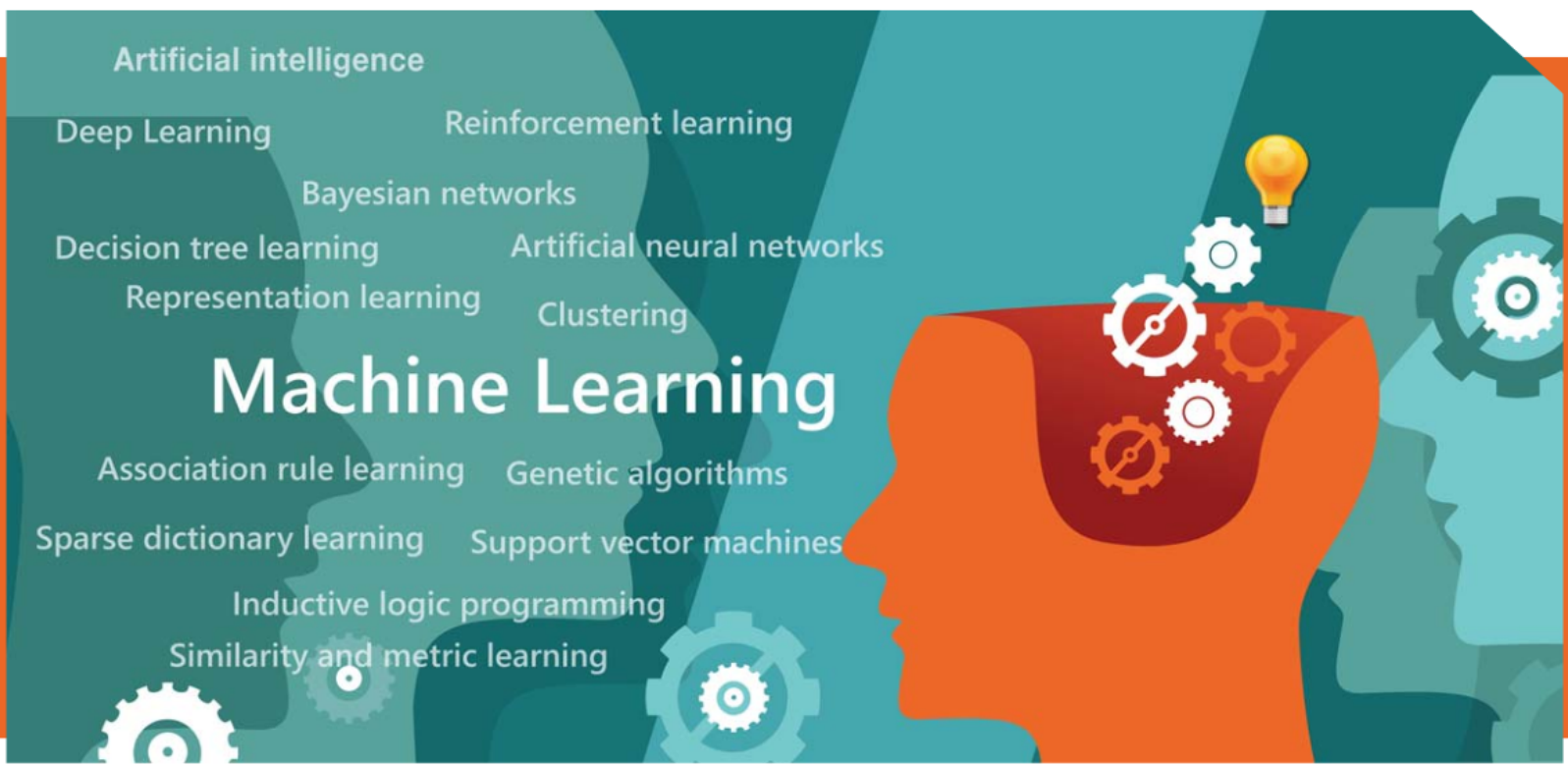

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FD-SOI Process Yields Rich Graphics on a Power-Sipping IoT Budget

IoT finds new life with technology that adapts to the often intermittent, bursty high-performance followed by periods of ultra-low power that IoT set-ups may often demand.

By Joe Yu, NXP

For Internet of Things (IoT) devices, proficient energy management and ultra-low power consumption are critical. One area of concern for conserving power lies within the IoT device's embedded processor.

The main factors contributing to the power efficiency of the processor include:

- Technology node
  - Wide dynamic voltage range
  - Low leakage
- Architecture
  - Heterogeneous processing
  - Power Islands
  - Power mode enablement

Of all the parameters, the process technology is fundamental to power efficiency. One recent process technology that has dramatically improved the landscape for power efficiency is Fully Depleted Silicon On Insulator (FD-SOI).

PROCESSOR TECHNOLOGY AND CORE ARCHITECTURE

Shrinking process technologies allow for higher integration along with lower run time power at a cost of increased static power due to higher leakage.

FD-SOI can prevent the trend of growing leakage through the following methods:

- Leveraging existing manufacturing techniques to apply an ultra-thin buried oxide layer on top of the silicon base (see Figure 1). The transistor channel is formed with a thin layer of silicon above the oxide layer. The buried oxide layer curtails the flow of electrons between the source and drain, which naturally reduces leakage current.
- The thinner transistor channel also allows for the use of lower Vdd voltages through better electrostatic control.

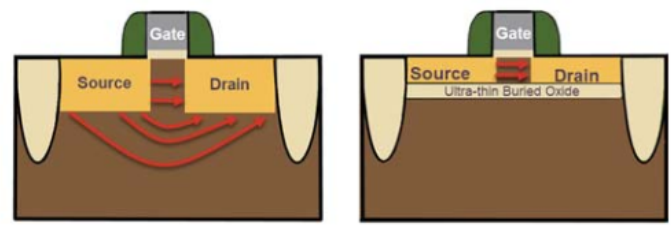

Figure 1: NXP has unique FD-SOI enablement in a large dynamic gate and body biasing voltage range, low quiescent current bias generators, and enhanced Analog-to-Digital Converter (ADC) performance.

Additionally, FD-SOI's ability to Reverse Body Bias (RBB), applying a negative voltage on the back side of the channel, can create a barrier preventing the movement of electrons.

Even though the shrinking process technology naturally allows for lower dynamic currents, FD-SOI can go a step further in reducing dynamic power through the following:

- Wide Vdd voltage range, allowing for operation at very low power levels.
- Forward Body Biasing (FBB) reduces the operating Vdd voltage for a given frequency. Instead of impeding the movement of electrons due to RBB, now electrons are encouraged to move.
- FD-SOI construction results in lower parasitics, lowering the dynamic power of the transistor.

As process technologies have gotten smaller, other trade-offs have arisen. Indeed, designing for analog signals has become more complicated. However, FD-SOI relaxes density rules, allows higher gain, a closer match of components (which reduces the need for compensation during layout), and achieves lower 1/f noise[1].

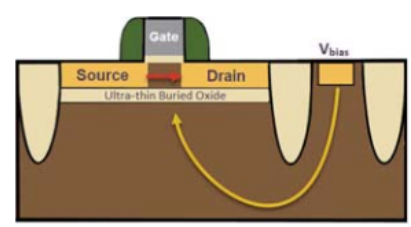

Figure 2: Body-biasing means that the device can be faster when required and more energy efficient when performance isn't critical.

1: Note that 1/f noise is found in electronics, music, nature, and other areas, and cannot be filtered out of an analog circuit. Chopper stabilization can be used but introduces switching noise.

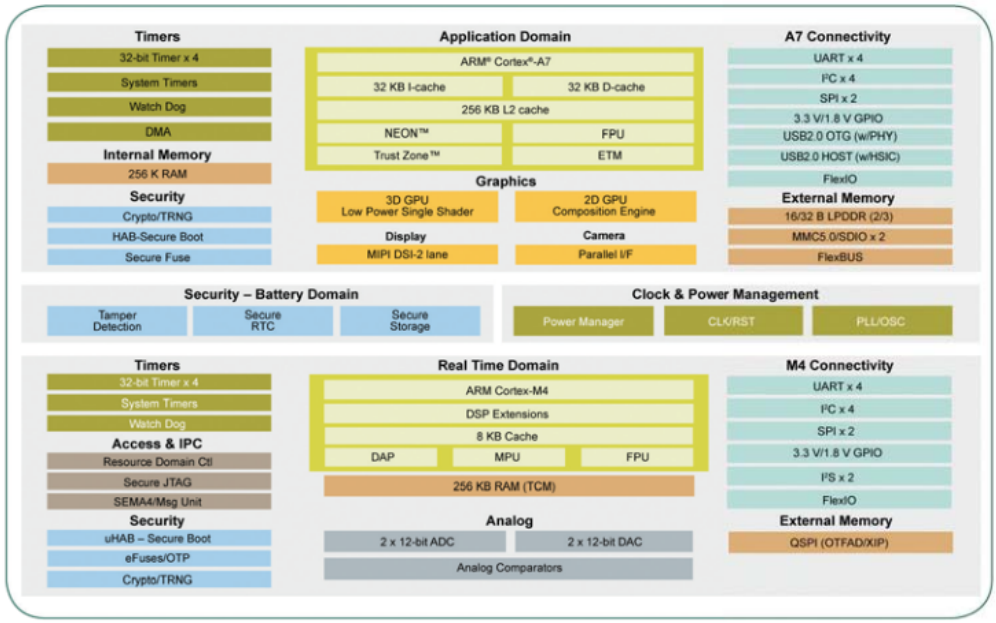

Figure 3: The i.MX 7ULP block diagram. The i.MX 7ULP is extremely flexible, with the ability to dynamically transition from high-performance to ultra-low power consumption while maintaining active operation. Bursty performance increases can be applied as needed, to offer the best of both worlds, which is especially relevant to IoT applications. (Image: NXP Semiconductors)

The industry is hitting a physical wall as miniaturization continues to approach ever-smaller nanometer nodes.

The physics of electricity at nanometer scale have begun to interfere with our design dreams of better, faster, smaller, cheaper, and more power-efficient chips. The smaller the architecture, the more significant the potential is for latch-up, as transistors within integrated chips are spaced physically closer to each other. Latch-up provides a potentially catastrophic alternate path for current flow, and until power is cycled to the chip, latch-up is present even after the condition that caused it is no longer present. However, the ultra-thin buried oxide layer utilized in the FD-SOI process provides immunity from latch-up.

FEATURES ENABLED BY FD-SOI

Taking a markedly different approach than do vendors who rebrand cell phone or tablet chips as 'IoT SoCs,' NXP has designed the new i.MX 7ULP applications processor from the ground up as an IoT device—choosing a low-power 28nm FD-SOI process node, a set of power-sensitive peripherals, and an architecture featuring dual power domains based on the Cortex-A7 and the Cortex-M4 cores.

By leveraging the process technology, power friendly heterogeneous architecture, and multiple smart power modes, the processor can achieve impressive ultra-low power consumption levels, with a deep sleep suspend of 50 µW or less.

The i.MX 7ULP offers Rich OS support (Linux, Android), as well as sophisticated Real-Time Operating Software (RTOS) support (FreeRTOS), and additional features suitable for IoT or any portable use case that demands long battery life.

The i.MX 7ULP family of processors is faster when required and more energy-efficient when performance is not as critical, enabling dynamic trade-offs. Engineers no longer face a forced selection: low-power processor or high-performance processor. Rather, the selection for performance or power efficiency can be made instantaneously, as needed, without having to reconfigure.

The i.MX 7ULP is well-suited for IoT edge devices, as well as smart home controls, building automation, portable patient monitoring, wearables, and portable scanners. The iMX 7ULP reaches a new level in IoT by offering the high performance required for rendering rich graphical images on a power-sipping wearable.

The IoT bestows upon nearly every industry the promise of significant forward progress by granting access to data at levels heretofore unseen. Harnessing the benefits of knowledge gained through the IoT is not going to be free or arrive without hazard. Yet seeking ever-higher productivity, with the potential to progress from the unknown to the well-informed, and in acquiring a new vehicle with which to spark innovation, we can't help but proceed.

Joe Yu is the Vice President and General Manager of the Low-Power MPU & LPC MCU product lines at NXP Semiconductors. He has been in the semiconductor industry since 1988 working for companies including NXP/Philips, Freescale, Toshiba, Altera and Atmel. Yu's work experience includes applications engineering, marketing, business development as well as general management. His passion is to develop low-power microprocessors and microcontrollers for broad market applications. As greater levels of processing and connectivity push to the edge nodes, one of the key areas of focus he has been championing is to find new ways to reduce the power consumption of these IoT devices. Yu has a BSEE degree from Santa Clara and resides in Palo Alto, CA.

Emerging Applications Spell the End of the Battery's Life

New mobile applications, such as wearables and mobile gaming, mean there is a shift in power management at the system level, seeing alternative ways to meet performance levels and design challenges.

By Caroline Hayes, Senior Editor

Applications such as autonomous driving and artificial intelligence are driving a demand for higher performance, high efficiency processors. These rely on processing images in real time and dissecting each image to identify and locate an element within that image to detect objects or to learn behavior.

Image processing and image recognition offer the possibility of creating new operations in other markets. Nick Pandher, Director of Market Development for Radeon Professional Graphics, at AMD, believes we are only seeing the tip of the graphics processing iceberg for deep learning. For example, he suggests, they could be used in financial institutions and organizations to model a training framework in a financial data set. This would perform the analysis usually done by someone with a financial background. It can also be used to look for anomalies in staff log-ins to flag issues and highlight at-risk areas in an organization's operations.

There are also medical uses for treatment, where anomalies can be quickly identified, and in research, where patterns can be detected across multiple data frameworks to link symptoms.

POWER ADOPTS A GAME FACE

AMD has based its latest Graphics Processing Unit (GPU), Radeon Mobile, on a 14nm FinFET technology, to meet the form factor and power demands of emerging markets, such as mobile gaming.

Mobile gaming places different demands on a GPU than a desktop application does. For example, for mobile, the GPU has to be light in weight and small in size to integrate into mobile devices or Virtual Reality (VR) headsets. It has to be thermally efficient, as a fan will add weight and space restrictions, yet have a laptop's performance.

FinFETs are 3D Field Effect Transistors (FETs), named after their fin-like structure rising above the substrate.

Figure 1: Mobile gaming is expected to account for half of the revenue generated by the video game industry worldwide by 2020. Picture Credit: AMD

The transistor's gate wraps around the fin to reduce the amount of current leaking when the device is in the off state. This approach lowers threshold voltages to improve power consumption without increasing the die size.

Scott Wasson, Senior Manager of Technical Marketing, AMD, confirms the reason for the choice of transistor: "The key thing for anyone building a chip like [Radeon Vega Mobile] is to keep voltage as low as you can. . . . Radeon WattMan [AMD's power management, based on Radeon software which controls GPU voltage, clocks, fan speed, and temperature], can be used to tweak and tune the voltage," he says.

By adding "a few bits of special sauce" to the earlier Polaris architecture, the company has improved switching speed and performance in the Vega mobile architecture, explains Wasson. "It is very important to be always the refining power management algorithms we build into hardware and software," he says. "The essential strategy is to provide performance when needed and to turn down the clocks, and the power, when you don't need the performance, in order to conserve power," he adds.

While the Vega Mobile, announced at CES last month, is not VR-ready yet, it is built to be small and relatively low power to meet the benchmark for VR in anticipation of what AMD's partners will develop for VR and mobile gaming.

WEARABLE CHALLENGES

For wearable devices, the same restrictions on weight, size, and power apply as in mobile gaming processors. They have to be light enough to be worn during fitness activities or light and unobtrusive if used in medical monitoring. For both, they should be wireless too, so that the wearer can record or gather data without being tethered.

Products such as watches, trackers, and monitors rely on a battery for power, but the processor's power system must be able to regulate voltage from the battery. The problem is that the battery runs down, so the system has to manage a source with a declining voltage output. Some wearable device functions need a higher voltage than the 3.2 to 4.2V typical of a rechargeable Lithium Ion battery. Many wearable products use main power rails that are below the minimum charge of a single cell Lithium Ion battery, so the rails are sourced by a step-down regulator, possibly more than one.

Maxim Integrated introduced the MAX14690 battery charge device last year (Figure 2), targeting low-power, wearable applications. It has a linear battery charger with a smart power selector, two low- power buck regulators, and three low-power, Low DropOut (LDO) linear regulators.

If the device is connected to a power source, the power selector allows the device to operate when the battery is dead. The input current to the selector is limited, based on an I2C register, to avoid overloading the power adapter. If the charger power source cannot meet the supply needs for the whole system load, the smart power control circuit can supplement the system load with current from the battery.

To conserve power during periods of light load operation, the synchronous step-down buck regulators have a burst mode option and a fixed frequency Pulse Width Modulation (PWM) mode to regulate the load. The output can be programmed using I2C bus.

The LDO linear regulators can also be programmed via I2C and configured to operate as power switches to disconnect the quiescent load of the system peripherals for power management.

This is all packed into a 36-bump, 0.4mm pitch 2.72 x 2.47mm Wafer Level Package (WLP). Maxim Integrated also offers the MAX14690 Evaluation Board, an assembled and tested circuit for evaluating the device.

"For wearable devices, the same restrictions on weight, size and power apply as in mobile gaming processors. They have to be light enough to be worn during fitness activities or light and unobtrusive if used in medical monitoring."

BATTERY MANAGEMENT IN THE IOT

The nature of the Internet of Things (IoT) means it has its own low-power requirements. Devices are wireless, mobile, often located remotely, and rely on batteries. In many designs, the battery is the sticking point. The battery can be expensive to replace. Additionally, the remoteness of the IoT node, either geographically, or in a hard-to-reach spot in a building or factory, can make battery replacement a time-consuming exercise. Hence the concentration by many Power Management Integrated Circuit (PMIC) manufacturers to take a system-level approach to power management.

The vision of the IoT is for hundreds of billions of nodes to be still active into the next century, despite being located in hard-to-reach, inaccessible, or hostile locations. For Dr. Peter Harrop, Chairman of market research firm IDTechEX, this means batteries will have to go (Battery Elimination in Electronics and Electrical Engineering 2018-20128). In a series of reports, he points out that batteries have "serious limita-

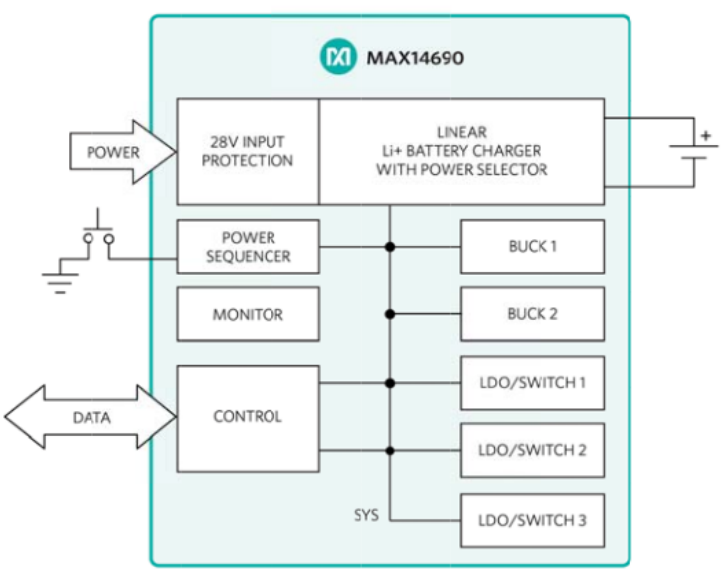

Figure 2: The MAX14690's level of integration minimizes footprint for power management in wearable devices.

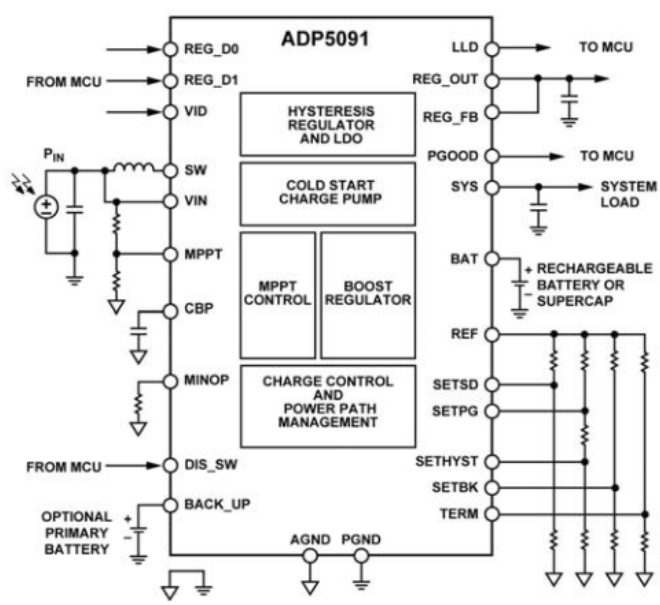

Figure 3: Analog Devices takes a system-level approach to IoT battery management.

tions of cost, weight, space, toxicity, flammability, explosions, energy density, power density, leakage current, reliability, maintenance and/or life." He is clearly not a fan. He continues "Lithium Ion batteries will dominate the market for at least 10 years, and probably much longer, yet no Lithium Ion cell is inherently safe and no Lithium Ion battery management system can ensure safety in all circumstances."

Figure 4: The 24-lead LFCSP ADP501 by Analog Devices could eliminate batteries in the Industrial IoT.

Energy harvesting is an alternative, practical approach to eliminating batteries. A Power Management Unit (PMU) converts DC power from one energy source to another. For example, the ADP5091 and ADP5092 (Figure 3), by Analog Devices can be used in PhotoVoltaic (PV) cell energy harvesting, ThermoElectric Generators (TEG) energy harvesting, industrial monitoring, and self-powered wireless sensor devices as well as portable and wearable devices.

The PMUs harvest from 6µW to 600mW, with an internal cold start circuit which allows input voltage down to 380mV. In both devices, the charging control function protects the rechargeable energy storage by monitoring the battery voltage with the programmable charging termination voltage and the shutdown discharge voltage.

There is the option to connect a primary cell battery, managed by an internal power path management control block. This enables the power source to switch from the energy harvester, rechargeable battery, and primary cell battery.

The company also offers the ADP509 evaluation board, based on the ADP509PMIC and the Alta Device PV cell. It includes a PV panel and power management to enable devices to be powered by energy harvesting.

Caroline Hayes has been a journalist covering the electronics sector for more than 20 years. She has worked on several European titles, reporting on a variety of industries, including communications, broadcast and automotive.

Ultra-Low Power Hands-Free Solution for Voice Powered Smart TV Remotes

How an innovative wake on sound technology optimizes battery life.

By Udaynag Pisipati, Vesper Technologies Inc.

Remember the story of Alibaba and the forty thieves? The thieves open a treasure chest with a voice trigger "Open Sesame" in the middle of a forest. I wonder if the captain of the thieves ever had to worry about battery replacement inside the treasure chest. But, that fictional voice interface experience is a perfect analogy for what modern day consumers expect to get out of their voice assistants. Unfortunately, the power-hungry nature of signal processing algorithms, if not tethering devices needing power to the wall, at the very least demands frequent charging.

A smart TV remote control with Push to Talk is one such use case that lacks the futuristic user experience of a voice activated TV remote due to the power constraints. Programming content on the TV is not so different from opening Alibaba's treasure, but a very complex task to execute using only keypad controls, given the numerous viewing options available both on broadcast as well as IPTV platforms. Finding a remote that is buried somewhere under the couch cushions and then discovering the specific program to view has always been a challenge, even for an average viewer, let alone less tech savvy or agile couch potatoes.

Hands-free voice functionality, therefore, is an indispensable feature to add to TV remote control, whether you want to catch up on your favorite news channel while sipping a cup of coffee in the morning or watch a movie on a Friday night lying on your couch with a bowl of popcorn. With rapid technological advancements in the Smart TV industry, it might appear that integrating far-field voice pickup into a smart TV is a viable option. For the TV to be always connected and using internet raises security concerns as well as challenges. These challenges include making a distinction between the user commands and TV playback and other background noises. And traditional always-on, always-listening solutions consume high standby power, thus eroding the battery life benefits achieved with the push-to-talk option on current voice remotes.

A typical TV remote with a push-to-talk feature has a battery lifetime of six months to one year for normal everyday operation. A seamless user experience along with a battery life comparable to that provided by current push-to-talk solutions on a voice remote is the need of the hour for the TV industry. Do we have to invent the wheel to find an alternate for an always listening solution? Not necessarily, as already on the market are technologies which offer simple but power-efficient solutions that can solve the battery life challenges for a hands-free remote.

CHALLENGES

One example of a way to replace push-to-talk remotes with an always listening solution is Zero Power Listening™ technology from Vesper Technologies. This solution uses a capacitive MEMS microphone to build a far-field voice remote. Such a design will continuously run a Voice activity detector to detect voiced versus non-voiced frames based on the speech activity level, as shown in the large dashed box in Figure 1. The active voice frames then trigger the rest of the system beginning with a wake word detection engine to identify if a wake word such as "Alexa" is spoken.

Once a wake word is detected, the voice command that follows the wake word is transmitted over a low energy transport protocol such as Bluetooth Low Energy, Zigbee etc. For the Voice activity detector to

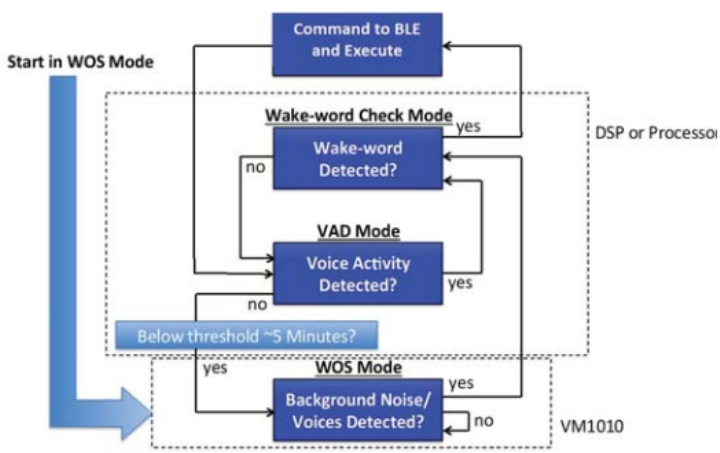

Figure 1: Flow chart for Wake word detection using Wake On Sound Mode

continuously monitor the systems, microphones at the front end need to operate in standby mode, consuming 200 µA on average, even when there is no sound to be heard.

Total system standby power, from Voice Activity Detect (VAD) to wake word check and command execution, therefore accumulates to the order of milliamps. In addition, the need for a microphone array to achieve high response accuracy in far-field scenarios only multiplies the standby power consumption of the entire system. Wake word detection therefore becomes the only bottleneck for a system with low power transport such as Bluetooth Low Energy that only consumes 0.1µA on standby. A push-to-talk system on the other hand is only active when the user presses the microphone button, thereby consuming very little overall power during command processing. For a far-field remote to operate with a long-term battery life, we need microphones with ultra-low power consumption in standby with a fast wakeup and a simple detection logic to wake up the DSP on voice activity. Vesper's Zero Power Listening chimes in as a perfect solution for the challenges mentioned above.

Zero Power Listening is a new power optimized architecture for always-on listening systems with an ultra-low power sound detector. The technology is implemented in Vesper's VM1010 microphone, which switches between two modes based on the acoustic activity in the environment:

a. Wake on Sound (WoS) mode with a current consumption of only 8µA where it is looking for sound activity that exceeds a certain sound pressure level (SPL) threshold within the voice band
b. Normal mode with a current consumption of 85 µA once a sound activity is detected.

The additional Wake on Sound mode in VM1010 acts as an acoustic watchdog to wake up the rest of the processor when there is a sound activity in the environment (Figure 1). In other words, WoS mode runs below the lowest power voice activity detect mode. In a noisy environment the system will move into voice activity detect mode. The threshold configuration between 65 – 78 dBSPL(A) provides an additional adjustment to control the WoS mode based on the expected acoustic level in the surrounding environment. In the case of a voice remote where the user is located at distance of 1-2m from the remote and the remote itself is, for instance, on a couch another 2m from the TV, the threshold provides the flexibility to fine tune the listening level of the microphone against the TV playback volume level. The minimum threshold level of 65 dB avoids false triggering from non-speech activity within the voice band. For a remote-control scenario, the background noise from the TV playback is a major concern to avoid switching from WoS to normal mode operation. Therefore, the maximum threshold of 78 dB is an optimal solution to avoid false triggering in this case. Figure 2 shows the mode triggers recorded with WoS microphone in a 24-hour period, which indicates that the switching between two modes happens only during the most active periods of the day in a typical household. This selective triggering with WoS mode, therefore, saves standby power as the rest of the TV remote including converters, voice processors etc. is in sleep mode.

CASE STUDY

Figure 3 shows the charge depleted by a TV remote using ZPL technology compared to alternate listening solutions. For the case study, the activity from a VM1010 microphone in a 24-hour period is recorded and then used to calculate the power numbers with the assumption that two AA batteries (3V @2400 mAh) are used. The WoS mode saves 80 percent in total energy compared to an alternate listening

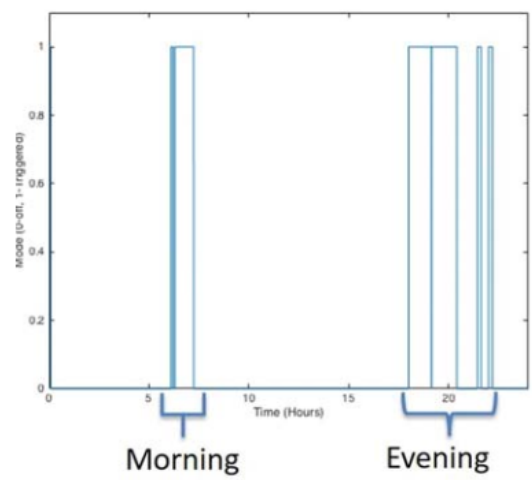

Figure 2: Logged data from VM1010 (x-axis shows time in a 24-hr period)

solution with capacitive MEMS microphones. On the other hand, the power consumed with the WoS microphone is also comparable to a push-to-talk solution. These savings in energy directly translate into battery life savings on the voice powered remote as shown in Figure 4. The WoS microphone increases the standby life of remotes by 10x and provides an overall battery life savings 4x times that of alternate listening solutions with a typical daily use.

The power savings obtained from the WoS remote are directly proportional to the number of wake on sound mode hours, i.e., the percent of time the TV playback level is lower than the wake on sound threshold in a day. Considering a TV playback time of three hours/day, Figure 5 shows that the WoS mode significantly increases the battery life by five times compared to when there is no WoS mode present, even

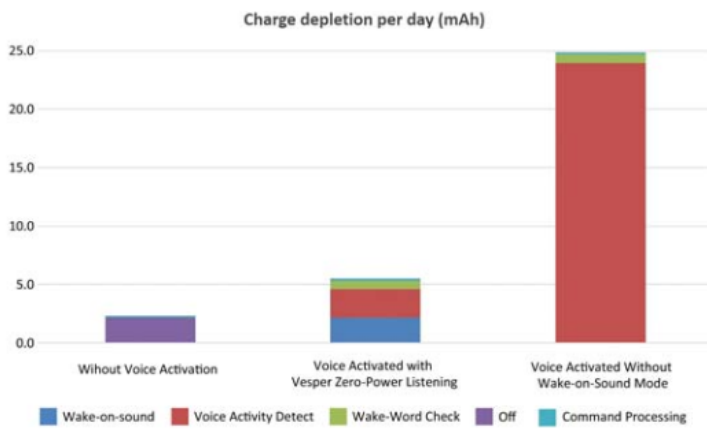

Figure 3: Energy depletion with Wake on Sound as compared to alternate listening solutions

when the VM1010 microphone is always in the normal mode during TV playback. These savings further improve as the wake on sound threshold is adjusted so that the microphone is in normal mode for half the time of TV playback.

Vesper's piezoelectric microphones also offer additional advantages for the voice remote use case. Piezoelectric MEMS microphones have a quick startup time of 50 µsec, which is 1000x less than a capacitive MEMS microphone, enabling more keyword detection accuracy. Piezoelectric material is inherently resistant to environmental contaminants such as water, dust, and even kitchen oil or popcorn butter, thereby offering robust performance for the long term. With Vesper's ZPL technology, a far-field voice remote also eliminates the need for an Accelerometer in the TV remotes, which is used as a wake-up trigger to identify when a user picks up the remote to use the push-to-talk feature. Perhaps this could help in cost and BOM savings for the remote manufacturers. For additional details on Voice remote case study and Vesper's product portfolio, please reach out to info@vespermems.com

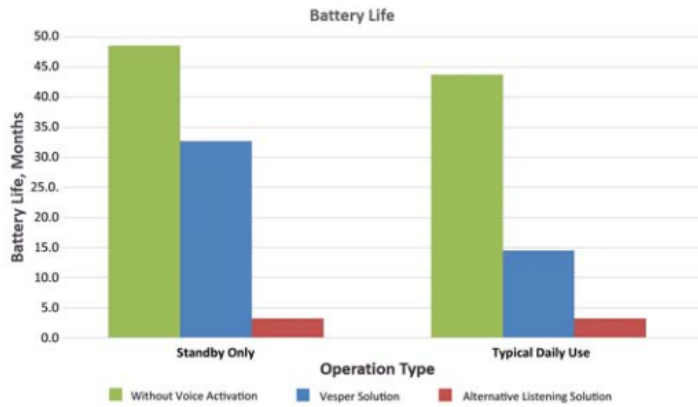

Figure 4: Battery life savings with Wake on Sound as compared to alternate listening solutions

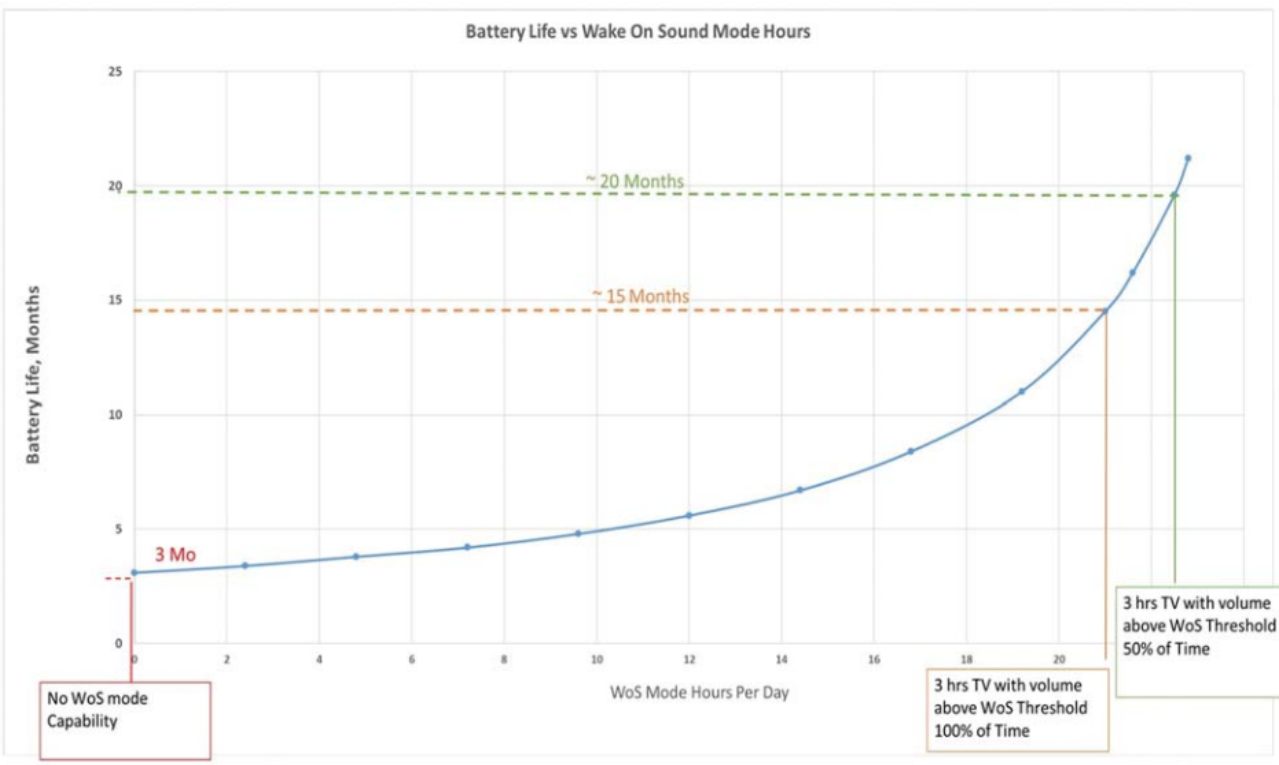

Figure 5: Battery Life Vs. Wake on Sound hours per day

Udaynag Pisipati is Sr. Field Applications Engineer at Vesper Technologies Inc. and has over 12 years of experience working in Speech/Voice applications for wireless devices. He holds a Masters degree in Electrical Engineering from University of Missouri - Columbia and an MBA from Santa Clara University. A firm believer in speech as a natural user interface for human-machine interaction, his areas of interest include everything related to speech processing such as Microphones/Speakers, Signal Processing and Machine Learning.

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RISC-V is Not a Company

By Lynnette Reese, Editor in Chief, Embedded Systems Engineering

RISC-V is a new open Instruction Set Architecture (ISA), named thus because it was the fifth RISC instruction set that had been developed. The highly flexible and extensible base ISA base was designed to be simple, clean, and suitable for direct hardware implementation. The base instructions are similar to other RISC instruction sets like OpenRISC or MIPS. RISC-V (pronounced "risk-five") is an open standard ISA that is royalty-free and free to implement. It's likely that there is not a significant marketing budget to establish awareness, so it's not surprising that some can mistake RISC-V for something else. However, RISC-V is not a company, and it is not a CPU. RISC-V began in 2010 as a project at UC Berkeley by Krste Asanović, Professor in the EECS Dept. at the University of California, Berkeley, current Director of the ASPIRE lab, and Chief Architect at SiFive. Asanović wanted a simple ISA without legal issues related to intellectual property. UC Berkeley began using RISC-V in engineering courses.

According to the RISC-V Overview in the RISC-V specifications, RISC-V is "a completely open ISA that is freely available to academia and industry; a real ISA suitable for direct native hardware implementation, not just simulation or binary translation; and an ISA that avoids "over-architecting" for a particular microarchitecture style (e.g., micro-coded, in-order, decoupled, out-of-order) or implementation technology (e.g., full-custom, ASIC, FPGA), but which allows efficient implementation in any of these." There are many open source projects based on the RISC-V ISA.

In 2015, RISC-V was officially kicked off by the newly formed RISC-V Foundation as a zero cost, royalty- and paperwork-free ISA. The mission statement of the RISC-V foundation is "to standardize, protect, and promote the free and open RISC-V instruction set architecture and its hardware and software ecosystem for use in all computing devices." Rick O'Connor is the executive director of the RISC-V Foundation.

The RISC-V Foundation, with more than 100 members, believes that the RISC-V ISA has potential to dominate the computing world from embedded and small form factor, all the way to warehouse data servers. The foundation creates and manages working groups to guide future development of the architecture. RISC-V Foundation members include Berkeley Architecture Research (BAR), Esperanto Technologies, Google, Microsemi, Nvidia, Qualcomm, Western Digital, IBM, IDT, Lattice, NXP, Samsung, Express Logic, Huawei, Siemens, Lawrence Berkeley National Laboratory, Mentor, Segger, and at Princeton, IIT Madras, and National Singapore Universities.

An ISA is a critical interface where hardware meets software. There seems to be a consensus on instruction sets these days. No one has built a new commercial Complex Instruction Set Computers (CISC) ISA in more than 30 years, and there is widespread agreement that the RISC architecture is best for general-purpose ISA. However, although there seems to be a lot of open source or open standards in many other areas, until recently, there has been no open source ISA for open and free implementation. RISC-V is set to fill the void.

Today, there are three different RISC-V instruction sets with address sizes in 32-, 64-, and 128-bits. Perhaps 128-bit addressing is deemed unneeded by some. However, the 128-bit ISA was created to ensure that RISC-V could successfully go there, and in reality, seems to have some application in addressing for huge flash drives and in security. The RISC-V base ISA has a minimal instruction set of less than 50 hardware instructions. There are also some optional standard extensions that include integer multiply and divide, atomic memory operations, compressed instruction encoding to make code size smaller, and single-, double-, and quad-precision floating point. RISC-V reserves opcode space for the unique instructions of SoCs, if needed. RISC-V is the smallest IA for 32- and 64-bit addresses. On average, RV32C, the compressed version of the 32-bit RISC-V instruction set, is 34% smaller than other 32-bit ISAs and RV64C (RISC-V 64-bit compressed) is 42% smaller than other 64-bit ISAs.

WHAT IS AVAILABLE FOR WORKING WITH RISC-V?

There are several RISC-V ISA specifications available online, including user level, privileged and compressed RISC-V instruction

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set specifications. The RISC-V toolchain is a standard GNU cross compiler toolchain (GCC/glibc/GDB) ported for RISC-V. RISC-V supports Linux (or...Linux supports RISC-V). RISC-V is also found in Yocto, and there is a verification suite. One of the best hardware tools for RISC-V, widely used in the universities, is Chisel. Chisel is a hardware construction language using a scala-embedded metaprogramming language. Chisel simultaneously produces a software simulator, an FPGA emulation, and a GDS Layout. Chisel is ideal for reuse (shared lines of code), and a BSD-licensed open source tool that's available at https://chisel.eecs.berkeley.edu/.

The time is right for an open ISA with a standard base. Sun created one years ago, but it faded. The continued rise of SoCs seems to have reinitiated the attractiveness of an open ISA that wasn't as strong with the Sun attempt. Moore's law is ending which means we will be moving to domain specific architectures. The definition of an ISA is that it is a vital interface where hardware meets software. Additionally, after several decades, computing seems to have reached a consensus favoring Reduced Instruction Set Computers (RISC). Even Complex Instruction Set Computers are using RISC "under the hood." Nevertheless, ISAs add a necessary but considerable amount of cost to computing. To port software from one ISA to another is expensive. There are many different ISAs for the many Systems-on-Chip, but ISAs do not affect system performance or energy efficiency as much as algorithms, compilers, circuit design, or fabrication processes, making RISC-V a good candidate for open and free implementation.

THE CASE FOR RISC-V

RISC-V can provide a shorter time-to-market, fewer errors given more developers are looking at it, lower cost from reuse, and transparency that makes it difficult for governments to add secret trapdoors. Arm has no fabrication plant, and yet is nearly ubiquitous in smartphones and beyond. Arm has successfully proven that a company can sell the IP for an instruction set or processor and others will fabricate it. It is much easier for designers to take an open ISA and change it or add proprietary sections for reuse.

An industry-standard ISA lends itself to a larger population of engineers with collective experience, a vibrant ecosystem, and community forums forming around a shared basis. Architecture research and education would be more realistic and able to leverage fully open hardware and software stacks. Open source makes products such as the Internet of Things less expensive. RISC-V can span the small to the large in computing. Historically, standards bodies have cooperated together for many other open technologies, but not an ISA. Until now.

Lynnette Reese is Editor-in-Chief, Embedded Intel Solutions and Embedded Systems Engineering, and has been working in various roles as an electrical engineer for over two decades. She is interested in open source software and hardware, the maker movement, and in increasing the number of women working in STEM so she has a greater chance of talking about something other than football at the water cooler.

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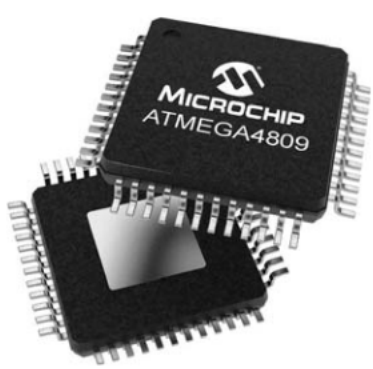

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